Design of Binary to BCD Code Converter using Area Optimized Quantum Dot Cellular Automata Full Adder

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Abstract

The Integrated Circuit Technology (IC) is growing day to day to improve circuit performance and density for compact systems. A novel technology, Quantum dot Cellular Automata (QCA) was introduced to overcome the scaling limitations of CMOS technology. In order to bring a new paradigm of IC design in an efficient and optimized manner, a binary to BCD code converter is designed using QCA technology based area optimized adder. It is observed that the proposed binary to BCD code converter design gives better results in terms of the area and number of QCA cells. The results obtained by the proposed design shows that 61% of area reduced compared to boolean expression based design, this design is further optimized to reduce the QCA cell count by 45% with respect to the design in [1].

Keywords: ODE Converter, Quantum Dot Cellular Automata, Clock Zones, Wire Crossover, Majority Gate.

1. INTRODUCTION

The performance and density of IC technology is increasing successfully with CMOS devices for past few decades, but at nanometer scale they are facing new challenges such as short channel effects like drain-induced barrier lowering, punch-through, velocity saturation, hot carrier effects, sub-threshold   leakage currents etc. [2]. To overcome the limitations of CMOS technology, alternative nano electronic technologies have been proposed by researchers to invent a new technology which can work at nanometer dimensions; in those the International Technology Roadmap for Semiconductors (ITRS) has identified new technologies to replace the transistor based technology in future. Few of them are Resonant Tunneling Diodes (RTD), Quantum dot Cellular Automata (QCA) and Single Electron Transistor (SET). Out of all these technologies QCA seems to be suitable novel computing technology to replace the conventional CMOS technology [3].

QCA technology was proposed by Craig S.Lent et al, in 1993 [4] as an alternative technology to replace conventional CMOS technology. The QCA paradigm is based on quantum dots which is more suitable for logic circuits with very high performance and low power dissipation at nanometer scale. The QCA creates general computing systems at nanometer scale by encoding the binary data with the positions of two electrons. Using this principle QCA technology solves series of problems which exist in traditional circuit implementation at nano-scale. In recent years QCA technology has gained lot of popularity due to the interest in creating computing devices and any logic function implementation at nano-scale.

The main advantages of QCA technology over conventional CMOS technology are as following:
1) high density (~ 10) [5];
2) very high operational frequency (terahertz range) [6], [7];
3) low-power consumption (~ 100) [8].

In this paper, a full adder unit is optimized using a corner cell based QCA inverter. The adder-subtractor implemented using an area optimized 1 bit adder module. Further a binary to BCD code converter designed with 1 bit adder and compared the results with previous works via the metrics cell count, area and clock cycles [1], [9].

The rest of the paper is organized as; the section 2 briefly covers an introduction to QCA, clocking schemes and wire crossovers. Section 3 covers about previous QCA adders and binary to BCD code converter. The details of proposed area optimized QCA full adder, implementation of area efficient binary to BCD code converter and adder-subtractor using an area optimized full adder is presented in section 4. The section 5 covers the comparison of performance metrics in proposed designs with conventional adder and binary to BCD code converter. Finally conclusions are presented in section 6.

2. QCA BACKGROUND

In QCA technology primitive element is QCA cell as depicted in Figure. 1(a), contains four quantum dots placed at the corners of a square cell (18nm X 18nm). Quantum dot is normally 5nm diameter single electron container. Two electrons are injected into a QCA cell and they occupy two diagonal quantum dots in the cell keeping maximum distance due to columbic repulsion between each other. Electrons in one diagonal position can change to other diagonal position and these two directions are two polarizations, if electrons are present as shown in Figure. 1(b) polarization -1, which represents binary '0', and if electrons are as shown in Figure. 1(c) polarization is +1, which represents binary '1' [10]. There are three types of quantum dots to implement QCA circuits. 1) Metal-island quantum dots [11], [12]; 2) Semiconductor dots [13], [14]; 3) Molecular dots [15], [16], Metal-island quantum dot was first fabricated to demonstrate QCA implementation. In this method dot was built as Aluminum Island. The experiments were carried out with 1μm metal-island [6].

Semiconductor quantum dots could be used to implement QCA circuits with same fabrication method of CMOS devices. However, the current semiconductor process has not yet reached as small as nano-scale. In this paper semiconductor dot method is used for simulation at clock frequency is 1GHz.

A proposed method, but not yet fabricated is single molecule quantum dot can have advantages such as 1) highly symmetric cell structure; 2) high density; 3) very high switching speed; 4) room temperature operation; 5) possibility of self assembly. There are some technical challenges, which include selection of molecule, interfacing the cells and clocking mechanism, which are to be solved before the implementation of circuits.

(a)   (b)   (c)
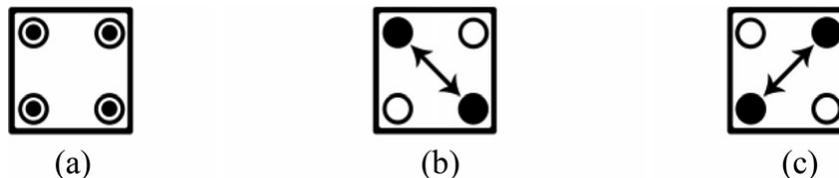
FIGURE 1: QCA cell: (a) empty cell, (b) polarization -1, (c) polarization +1.

2.1 Some of the QCA Wire and Basic Gate Models
1) QCA wire: An array form of QCA cells transmit binary information from one end to the other end, "1" or "0" which enters at first cell will reach to the last cell is called a QCA wire as depicted by Figure. 2(a) and 2(b) respectively.

2) QCA Inverter (QI): When two pairs shifted in horizontally or vertically becomes orthogonal and complements from one pair to other pair. For example an input logic "1" is shown to be inverted in Figure. 3(a). a robust QCA inverter with seven cells has been designed in Figure. 3(b) [17].

3) QCA Majority (QM) gate: QCA Majority gate is an important element in the implementation of circuits, and a primitive gate is the 3-input majority gate, which consists of five QCA cells in that three are input cells, one output cell and another center cell is an evaluating cell which find the majority of binary information from three inputs and transmits to the output cell [10]. For majority of inputs logic "1" and logic "0" as depicted in Figure. 4(a) and Figure. 4(b) respectively. If A, B, C are input variables and Y is output variable the majority gate expression is given by

$$Y=M(A,B,C)=AB+BC+AC \qquad\qquad (1)$$

If C=0 in eq. (1) then Y=AB i.e. if one input of majority gate is "0" then majority gate becomes an AND gate.

If C=1 in eq. (1) then Y=A+B i.e. if one input of majority gate is "1" then majority gate becomes an OR gate.
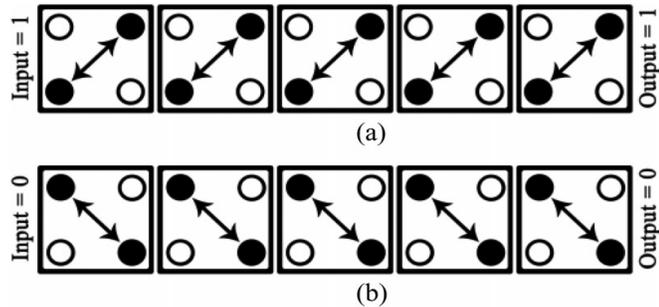
FIGURE 2: QCA wires: transmitting (a) "1" and (b) "0".
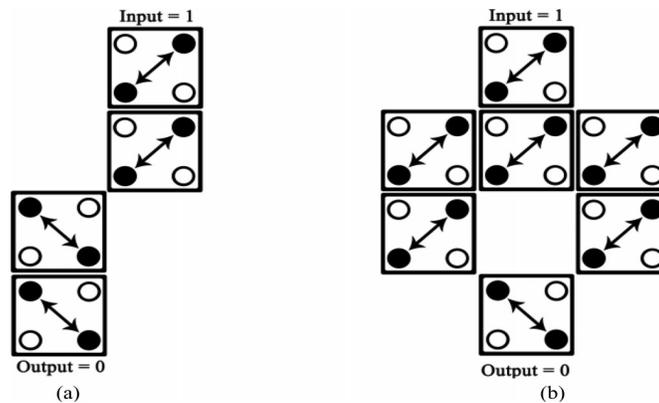
FIGURE 3: QCA Inverters: (a) Corner Inverter, (b) Robust Inverter.
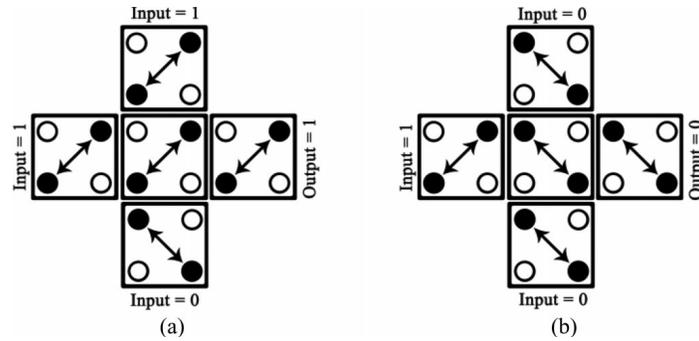
FIGURE 4: QCA Majority gates: (a) majority "1", (b) majority "0".

2.2 Wire Crossover
The intersection of two QCA wires is called as QCA crossover it is referred as QX. There are five types of crossovers 1) Multi-layer crossover in which two substrate layers are used to avoid interference [18]. 2) Coplanar crossover in which cells in one wire are 45˚ rotated [19], but it has less robustness and high implementation cost because of two types of cells [20], [21], [22]. 3) Multi-phase clocking crossover which uses three types of clocks with time division multiplexing [23]. However, it needs 8-phase clocking scheme which reduce the speed of transmission. 4) Logical crossover which uses XOR gates to avoid wire crossings. Nevertheless, it needs more area, latency is very high. 5) Clock-zone based crossover in which 180˚ phase difference between QCA cells in two wires to be intersected are used [24], [25]. It is very fast, robust and low cost crossover. A 4-phase clock scheme is used in this crossover.

2.3 QCA Clocking and Clock-zone Based Crossover
- QCA Clocking: There are four clock phases to QCA cells: 1) switch phase; 2) hold phase; 3) release phase; 4) relax phase as depicted in Figure. 5. [8], in the clock switch phase initially QCA cells are unpolarized and the potential barriers are low and they polarize in switch phase and their barriers become high; computation occurs in this phase. In hold phase of the clock, barriers remain at high. During the clock release phase, barriers go low and QCA cells become unpolarized. During the clock relax phase, barriers remain at low and QCA cells remain at unpolarized [26], [27], [28]. When clock is on the ground state interacts with excited states.
- Clock-zone based wire crossover: There are four clock zones in QCA cells, and they are clock 0 (green), clock 1 (pink), clock 2 (cyan) and clock 3 (white) as depicted in Figure. 6. Each clock zone differs by 90˚ with its adjacent or next clock zone and clock 0, clock 3 are adjacent each other. The intersection of two QCA wires can be implemented using 180˚ out of phase cells in two wires, so clock 0 and clock 2 can intersect to make a wire cross or clock 1 and clock3 can intersect to make a wire cross, two wire clock zone based wire cross and their signal transmission are depicted in Figure.7 (a) and Figure.7 (b) respectively.
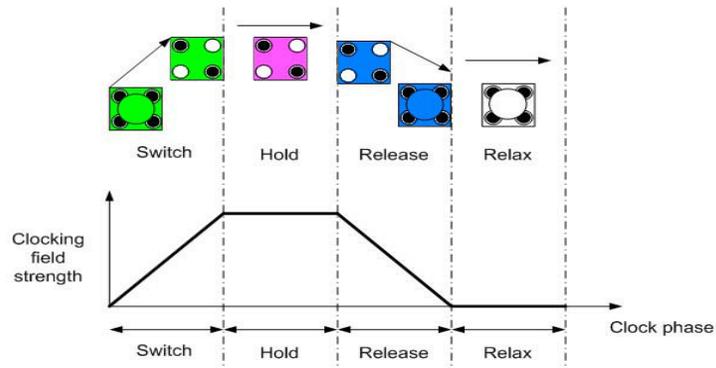
FIGURE 5: Four clock phases in QCA.

FIGURE 6: QCA cells four clock zones.
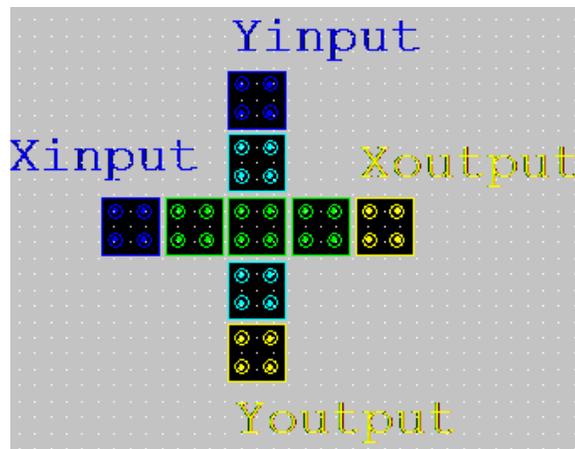
(a)
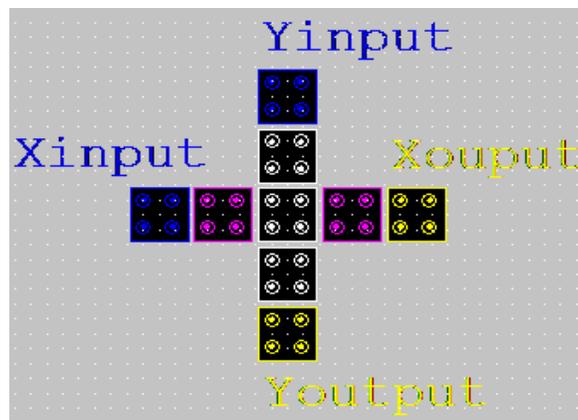
(b)

FIGURE 7: Clock-zone wire crossover: (a) clock 0, clock 2 crossover, (b) clock1, clock 3 crossover.

3. RELATED WORK

The previous work on QCA adders, Binary to BCD code converter is briefly described in this section.

3.1 QCA 1-bit Adders

A simple full adder description in terms of majority gate inverting functions, that found is [29], and as expressed by eq. (2), it can be realized with three QMs and two QIs

$$c_{out} = M(a, b, c_{in}), \quad sum = M(\overline{c}_{out}, M(a, b, \overline{c}_{in}), c_{in}) \qquad (2)$$

Here carry output majority function can be expressed in boolean function is
$c_{out} = ab + bc_{in} + ac_{in}$, sum function can be verified as follows

$$sum = \overline{c}_{out}(ab + b\overline{c}_{in} + a\overline{c}_{in}) + c_{in}(ab + b\overline{c}_{in} + a\overline{c}_{in}) + \overline{c}_{out}c_{in}$$

$$sum = \overline{c}_{out}(ab + b\overline{c}_{in} + a\overline{c}_{in}) + c_{in}ab + (\overline{a}\,\overline{b} + \overline{b}\,\overline{c}_{in} + \overline{a}\,\overline{c}_{in})c_{in}$$

$$= \overline{(a\,b + \overline{b}\,\overline{c}_{in} + \overline{a}\,\overline{c}_{in})}(ab + b\overline{c}_{in} + a\overline{c}_{in}) + c_{in}ab + \overline{a}\,\overline{b}\,c_{in}$$

$$= a\overline{b}\,\overline{c}_{in} + \overline{a}\,\overline{c}_{in}b + c_{in}ab + \overline{a}\,\overline{b}\,c_{in}.$$

3.2 n-bit QCA Adders

Following are the n-bit adders using a full adder, these adders were proposed in QCA and their brief description is given below.

- *Ripple carry adder:* This is very first QCA adders that we found in [3], where n full adders are used realize an n-bit adder.
- *Carry flow adder:* It is similar to ripple carry adder except that the delay in carry flow from input to output level reduced by ¼ clock cycles [30].
- *Carry look-ahead adder:* A QCA carry look-ahead adder design with 4-bit blocks are presented in [31], [32], [33], in which group generate and propagate signals were realized using QCA based AND, OR gates. Nevertheless, efficient uses of QMs for group generate signals realization [34].
- *Parallel prefix adder:* A parallel prefix adder would implement group generate, group propagate and carry signal with QCA based AND, OR gates, there are two QMs per a parallel prefix node. However, a parallel prefix node uses only one QM [32], whose left side input pair is the original one, here first level nodes are parallel prefix and last level nodes are Brent-Kung network.

3.3 Binary to BCD Code Converter

A binary to BCD code converter implemented in QCA technology [1], with three input majority gate and five input majority gate, the performance metrics compared with CMOS implementation. Later one occupies more than 1000 times area in comparison with QCA layouts.

4. AN AREA OPTIMIZED QFA, BINARY TO BCD CODE CONVERTER AND NEW ADDER-SUBTRACTOR

The main contribution is to design area optimized QFA based on corner based inverter, and we designed adder-subtractor and binary to BCD code converter using an area optimized QFA.

4.1. An Area Optimized QFA

We implement a QCA full adder using three QMs, two corners based QCA Inverters and two coplanar QCA crossovers (QX) [10] to optimize area and QCA cells. The block diagram representation of proposed full adder with majority gate, inverter blocks as depicted in Figure. 8(a). The QCA implementation of full adder is depicted in Figure. 8(b), there are 52 QCA cells; its latency is 1 clock cycle, with the area to $0.038\mu m^2$. The QCA layout simulated using

QCADesigner software [35], and simulation results in Figure. 9, depict the functional correctness of the full adder, and verified with full adder truth table described in Table 1. The simulation engine parameters are shown in Figure. 10. The performance of proposed full adder comparison with previous full adders for area, QCA cell count and wire crossover is described in Table 2. Full adders in [30], [36], [37] and [38] use multi-planar wire crossovers, full adders in [10], [39], [40] and our proposed adder use coplanar wire crossovers.

4.2 Proposed Binary to BCD Code Converter

We propose a new Binary to BCD code converter using an area optimized QFA presented in section 4.1, QMs, QI and clock-zone based QX [24], [25], used for the QCA implementation, where there are 260 QCA cells and area $0.28\mu m^2$. When binary code is converted to BCD carry will be generated, if decimal equivalent of binary number is greater than or equal to 10. To find BCD code "0110" will be added to binary number. The logic circuit and majority gate based block diagram for code converter are depicted in Figure. 11(a) and Figure. 11(b) respectively. The QCA layout and simulation results of binary to BCD code converter are depicted in Figure. 12(a) and Figure. 12(b) respectively. The performance of our new design is compared with previous designs in section 5.
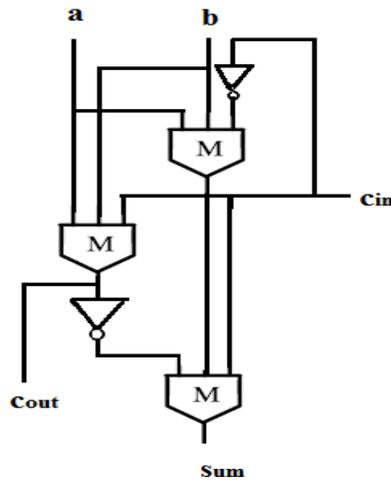
(a)
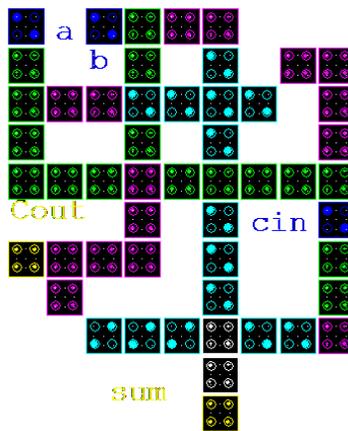
(b)

FIGURE 8: New QCA Full Adder: (a) Block Diagram, (b) QCA Layout.
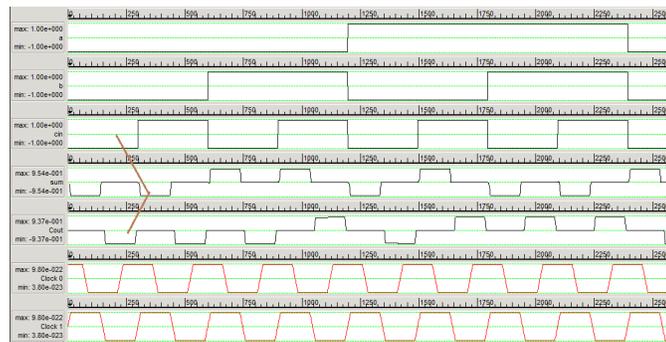
FIGURE 9: New QCA Full Adder Simulation Results.

FIGURE 10: QCADesigner Simulation Parameters.

Inputs			Outputs	
a	**b**	**c**	**Sum**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE 1: Truth Table of Full Adder.

QFA	Cell		Area		Latency (clocks)	Layer type
	count	Ratio	µm^2	Ratio		
New	52	1	0.038	1	1	Coplanar
[10]	59	1.134	0.043	1.131	1	Coplanar
[37]	95	1.826	0.087	2.289	2	Multiple
[30]	73	1.403	0.080	2.105	¾	Multiple
[39]	102	1.961	0.097	2.552	2	Coplanar
[40]	145	2.788	0.16	4.21	1	Coplanar
[38]	93	1.788	0.087	2.289	1	Multiple
[36]	79	1.519	0.064	1.684	1	Multiple

TABLE 2: Comparison of QCA Full Adders (QFA).
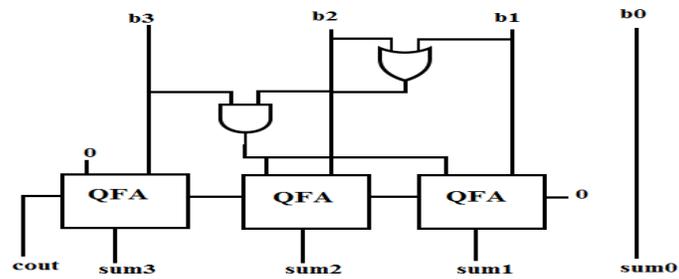
(a)
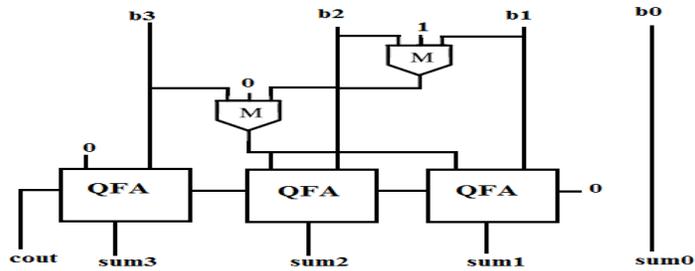
(b)

FIGURE 11: Binary to BCD Converter: (a) Logic Circuit, (b) QCA Block Diagram.

(a)

(b)
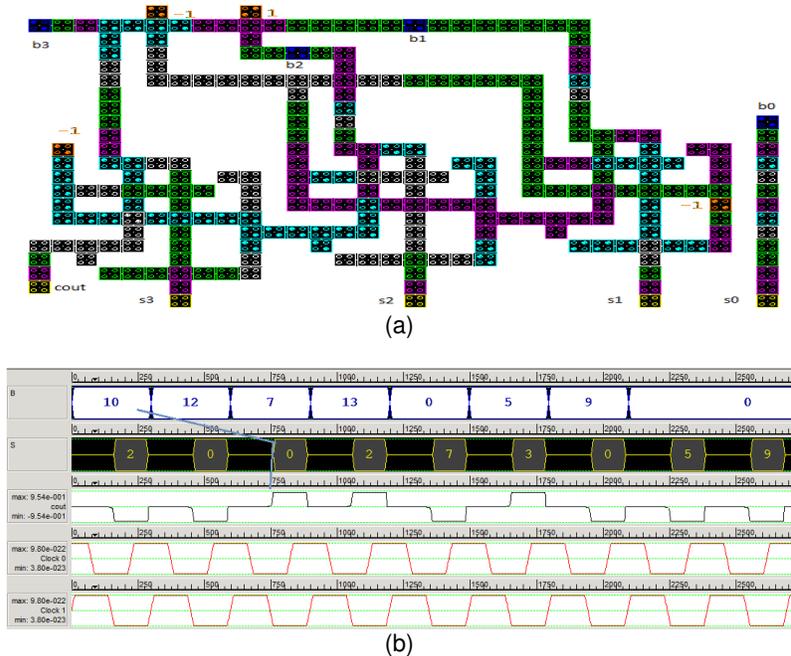
FIGURE 12: Binary to BCD Converter: (a) QCA Layout, (b) Simulation Results.

Binary to BCD converter	Cell		Area		Latency (clocks)
	count	Ratio	μm²	Ratio	
New	260	1	0.28	1	2.5
[1] with 3 i/p majority gate	512	1.969	0.76	2.714	3
[1] with 3 i/p majority gate	474	1.823	0.72	2.571	2

TABLE 3: Comparison of QCA Binary to BCD Code Converters.

4.3 QCA n-bit Adder-Subtractor

A new adder-subtractor proposed using an area optimized full adder. A QCA XOR gate used to find the 2's complement in subtraction, XOR gate logic symbol depicted in Figure. 13(a), XOR gate realized using one OR gate, two AND gates and one inverter depicted in Figure. 13(b). The QCA majority gate, inverter block diagram of XOR gate is depicted in Figure. 13(c). In QCA implementation of XOR gate there are 33 cells and 3 clock phases or ¾ clock cycles used as depicted in Figure. 14(a). The functionality of XOR verified with simulation results depicted in Figure. 14(b).

(a)

(b)

(c)
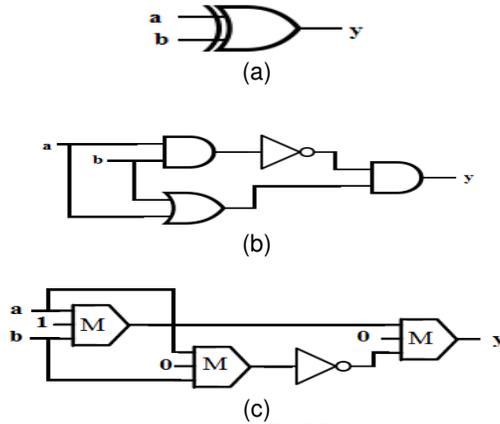
FIGURE 13: XOR gate: (a) logic symbol, (b) AND, OR realization, (c) majority gate realization.

(a)

(b)
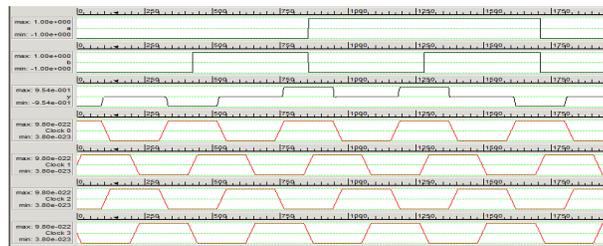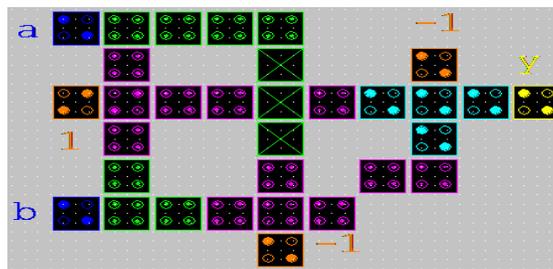
FIGURE 14: XOR Gate: (a) QCA Layout, (b) Simulation Results.

The QFA as shown in Figure. 8(a) can easily be cascaded to implement n-bit adders. We use an XOR gate for each full adder and proposed new n-bit 2's complement form of adder-subtractors. For n=4, a 4bit adder-subtractor block diagram with four full adders and four XOR gates depicted in Figure. 15(a), QCA layout implementation is depicted in Figure. 15(b), there are 472 cells, 0.48μm^2 area, 2.75 clock cycles used in layout design, and simulation results depicted in Figure. 15(c), shows the functional correctness of the QCA layout. For n=8 and n=16 QCA layouts implemented as depicted in Figure. 16(a) and Figure. 16(b) respectively. There are 971 cells, 0.95μm^2 area, 3.75 clock cycles in the QCA layout implementation of 8bit adder-subtractor and 2158 cells, 2.22μm^2 area, 5.75 clock cycles for 16bit adder-subtractor.

(a)

(b)

(c)
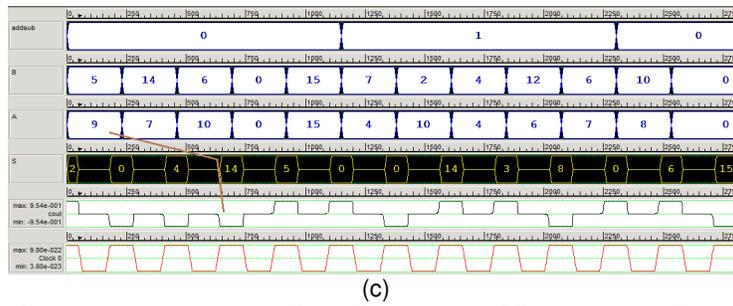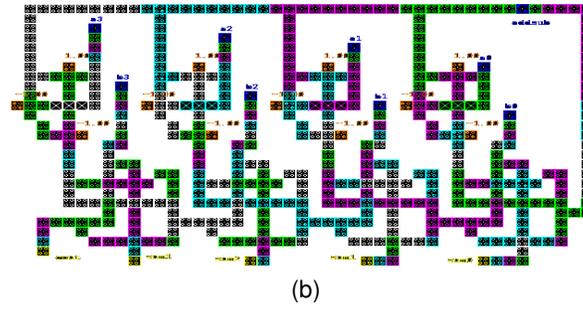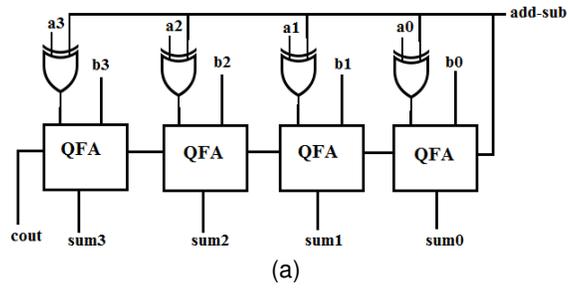
FIGURE 15: 4bit Adder-subtractor: (a) Block Diagram, (b) QCA Layout, (c) Simulation Results.

(a)

(b)
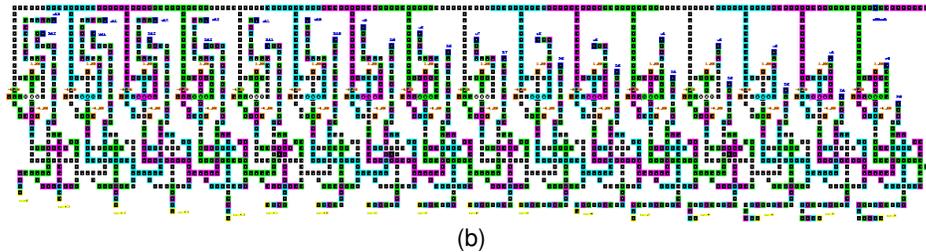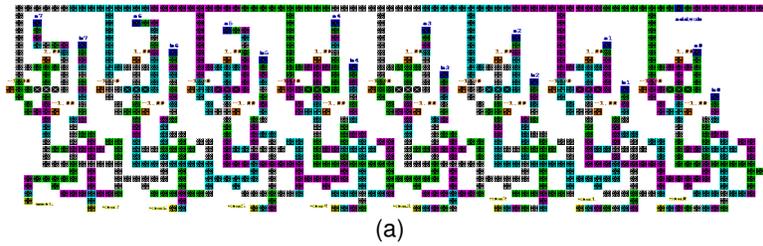
FIGURE 16: (a) QCA Layout of 8-bit Adder-subtractor, (b) QCA Layout of 16-bit Adder-subtractor.

5. PERFORMANCE EVALUATION AND COMPARISONS

We evaluate the performance of an area optimized QFA for the parameters are number of QCA cells, latency and area of the layout. The values of our implementation are compared with previous designs and presented in Table 2. In particular the cell count and area are reduced by 11% to 76% and 12% to 64% which shows the improvement in the new QFA.

The performance of proposed binary to BCD converter is compared with previous design and given Table 3. Comparison of results with results in [1] shows that cell count and area are reduced by 45% to 49% and 61% to 63% respectively.

The QCA cell count and area used to design a full adder in this paper are compared with previous results as shown in Figure17 (a) and Figure17 (b) respectively. The bar '1' in the charts is used for the representation of our results and bars '2' to '8' are used for previous results. It shows that the cell count and area reduced by 76% and 64% respectively.
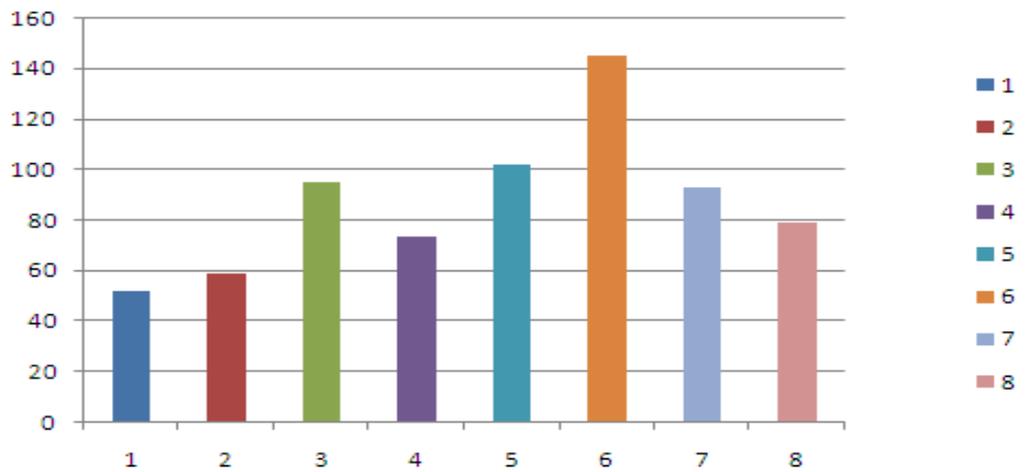
(a)
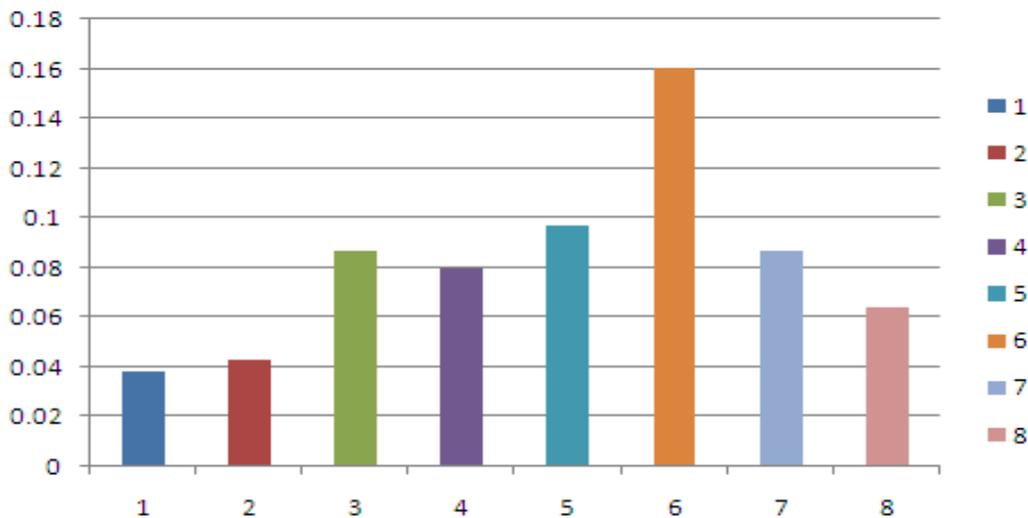
(b)

FIGURE 17: Comparison of QCA Full Adders for (a) Cell Count, (b) Area in μm^2 .

The results of QCA binary to BCD convertor are for cell count and area compared with previous results as shown in Figure18 (a) and Figure18 (b) respectively. The bar '1' in the charts is used for the representation of our results and bars '2' to '3' are used for previous results. It shows that the cell count and area reduced by 49% and 63% respectively.
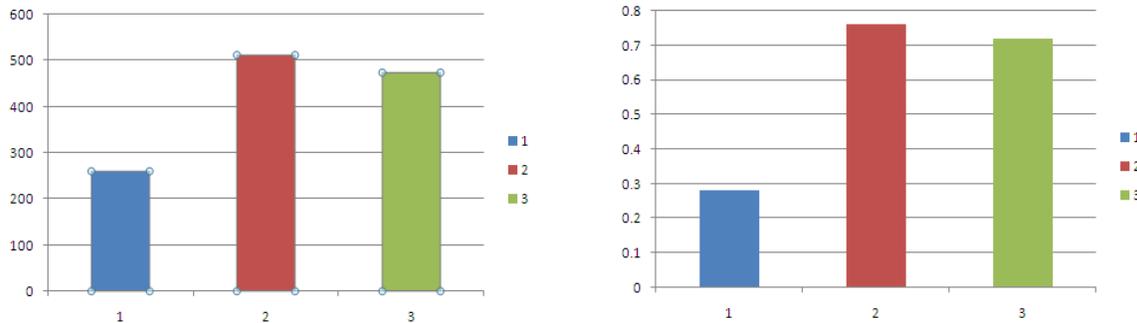
FIGURE 18: Comparison Binary to BCD Code Converters (a) Cell Count (b) Area in μm^2.

6. CONCLUSIONS

An area optimized QFA proposed using minimum number of cells with the latency of 1 clock cycle. It results an improvement in the performance of new design by reducing QCA layout area from 12 to 64% and cell count from 11 to 76%. This area optimized QFA is used to implement a new 2's complement based adder-subtractor for 4-bit, 8-bit and 16-bit data, the simulation results verified for their functionality.

A new Binary to BCD code converter in QCA technology is proposed to reduce area and cell count. We achieved 61% reduction in area and 45% reduction in QCA cell count.

This work can be extended to fabricate the QCA layouts using molecular or semiconductor quantum dots.

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