Design and Simulation of Moore Logic Circuit based SAR Analog to Digital Converter

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Abstract

In this work the circuit of 4 bit successive approximation Register Analog to digital converter is designed and simulated by using Multisim 11 program. Here the idea is to design a circuit that give low power consumption. The proposed circuit is designed with the sequential synchronous logic circuit idea by using Moore theory for the first time, so the state diagram is built and then implemented by using J-k flip flop, the proposed circuit is tested by DC and AC input voltages, so that the maximum voltage is 5 v and minimum voltage is 0 v, and so the step voltage will be 0.3125 v. SAR ADC needs Digital to Analog circuit, Latch circuit, and comparator which compare between the input voltage and the voltage results from the DAC, and all these circuits were built in this work with all they needs.

Keywords: ADC, SAR ADC, Logic circuit, Moore Sequential Model, Karnaugh Map.

1. Introduction

Over the past two decades, silicon integrated circuit (IC) technology has evolved so much and so quickly that the number of transistors per square millimeter has almost doubled in every eighteen months. Since the minimum channel length of transistors has been shrunk, transistors have also become faster. The evolution of IC technology has been driven mostly by the industry in digital circuits such as microprocessors and memories. As IC fabrication technology has advanced, more analog signal processing functions have been replaced by digital blocks. Despite this trend, analog-to-digital converters (ADCs) retain an important role in most modern electronic systems because most signals of interest are analog in nature and must to be converted to digital signals for further signal processing in the digital domain [1].

Analog-to-digital converters (ADC's) are often used to collect data from sensors, such as touchscreens, thermometers, camera image sensors and battery meters. To do this, the ADC measures the voltage or current input, and outputs a string of bits, which represents the input voltage or current. There are many applications for analog-to-digital converters, ranging from sensors, audio and data acquisition systems to video, radar and communications interfaces. The applications that require the highest sample-rates in the ADC are typically found in video, radar and communication areas [2,3].

2. Types of ADC

2.1 Flash ADC

Flash ADC conversion is the fastest possible way to quantize an analog signal. In order to achieve N-bit from a flash ADC, it requires (2^N-1) comparators, (2^N-1) reference levels and digital encoding circuits. The reference levels of comparators are usually generated by a resistor string. The high sensitivity of the comparator offset and a large circuit area are the main drawbacks of a flash ADC. For instance, to build a 10-bit ADC based on flash architecture requires more than 1,023 comparators. Therefore, it will occupy a very large chip

area and dissipate high power. Moreover, each comparator must have an offset voltage smaller than $1/2^{10}$, which is quite difficult to build [1].N-bit flash ADC is shown in FIGURE1. Here a resistive ladder drives a bank of (2^N-1) comparators, whose Logic encoded output is converted to a binary code with a binary encoder [4].

2.2 Digital ramp ADC

Also known as the stair step-ramp, or simply counter A/D converter, The basic idea is to connect the output of a free-running binary counter to the input of a DAC, then compare the analog output of the DAC with the analog input signal to be digitized and use the comparator's output to tell the counter when to stop counting and reset. The basic idea can be shown in FIGURE2-a, and the output can be seen in FIGURE 2-b.

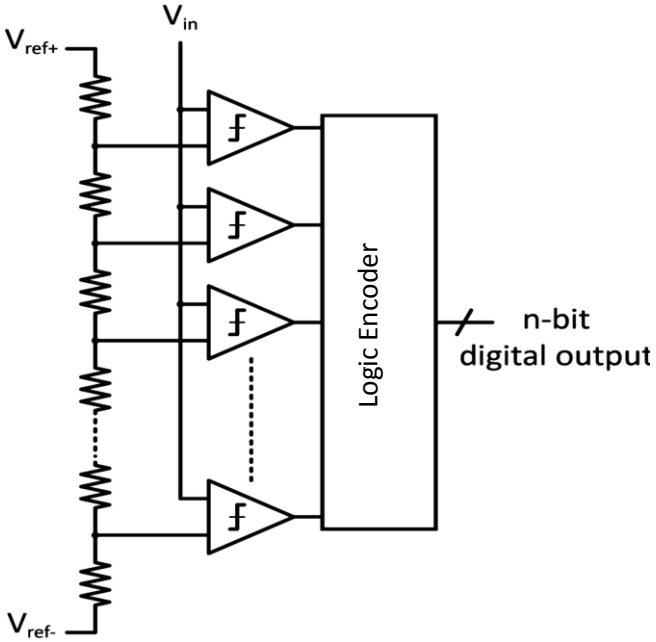
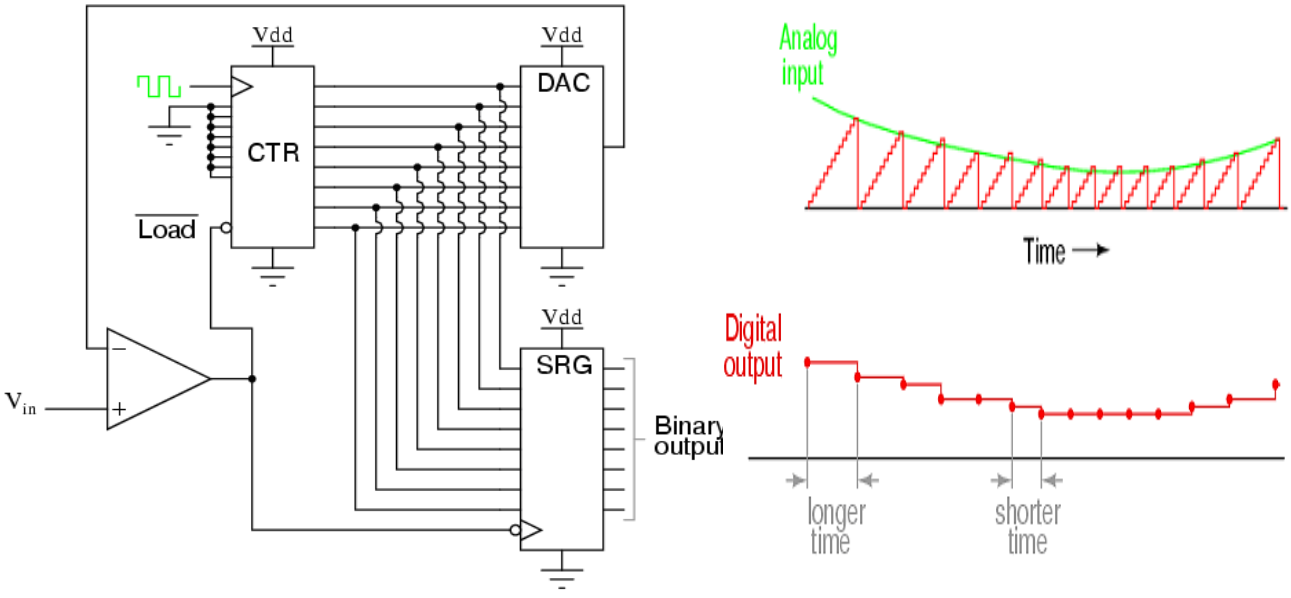


FIGURE1: N-bit flash ADC



(a) (b)

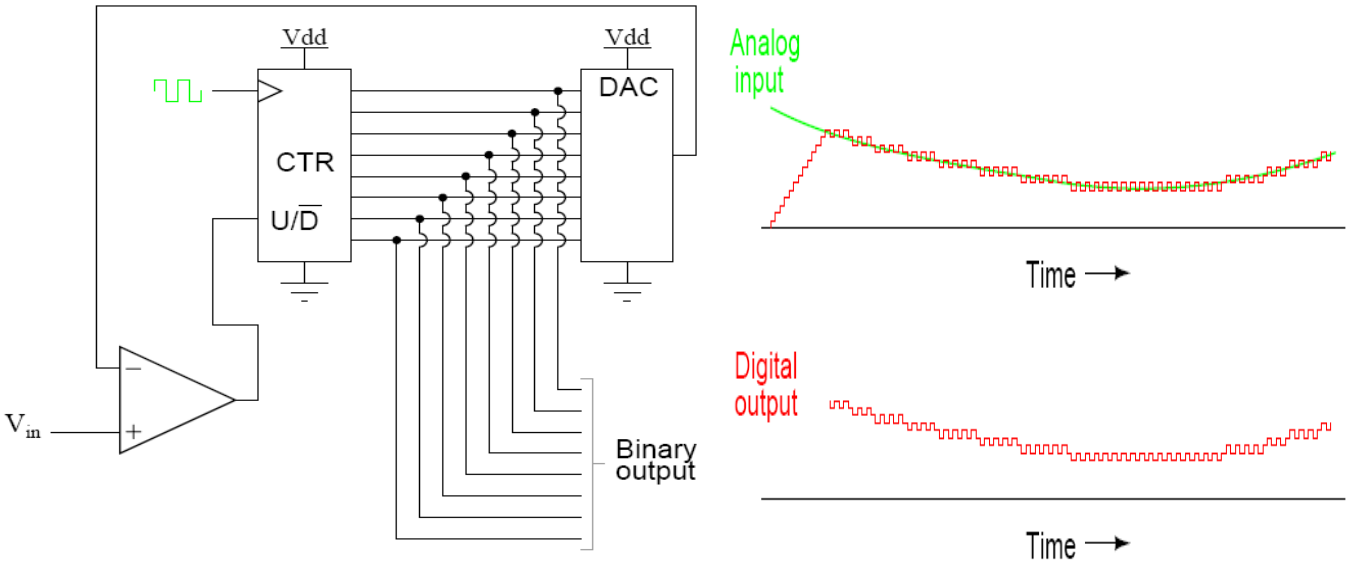
FIGURE2: a- Counter ADC. b- The outputs of counter ADC.

Note how the time between updates (new digital output values) changes depending on how high the input voltage is. For low signal levels, the updates are rather close-spaced. For higher signal levels, they are spaced further apart in time as shown in FIGURE2-b. For many ADC applications, this variation in update frequency (sample time) would not be acceptable. This, and the fact that the circuit's need to count all the way from 0 at the beginning of each count cycle makes for relatively slow sampling of the analog signal, places the digital-ramp ADC at a disadvantage to other counter strategies [5].

2.3 Tracking ADC

Here instead of a regular "up" counter driving the DAC, this circuit uses an up/down counter. The counter is continuously clocked, and the up/down control line is driven by the output of the comparator. So, when the analog input signal exceeds the DAC output, the counter goes into the "count up" mode. When the DAC output exceeds the analog input, the counter switches into the "count down" mode. Either way, the DAC output always counts in the proper direction to track the input signal. The circuit and output are shown in FIGURE3-a and 3-b.

Note that the much faster update time than any of the other "counting" ADC circuits. Also note how at the very beginning of the plot where the counter had to "catch up" with the analog signal, the rate of change for the output was identical to that of the first counting ADC. Also, with no shift register in this circuit, the binary output would actually ramp up rather than jump from zero to an accurate. Perhaps the greatest drawback to this ADC design is the fact that the binary output is never stable: it always switches between counts with every clock pulse, even with a perfectly stable analog input signal. This phenomenon is informally known as bit bobble, and it can be problematic in some digital systems [5].



(a) (b)

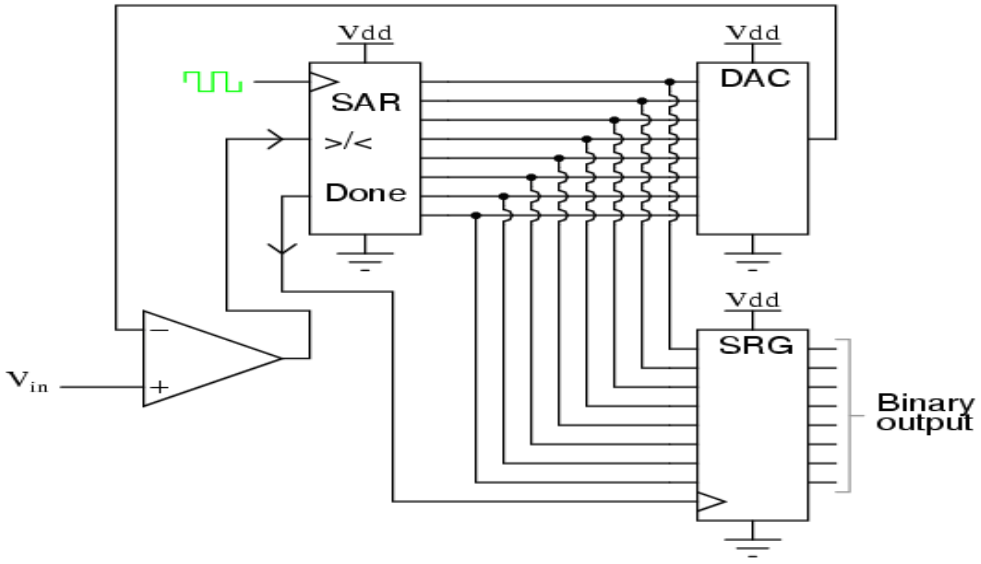
FIGURE3: a- Tracking ADC. b- The outputs of Tracking ADC

2.4 Successive Approximation ADC

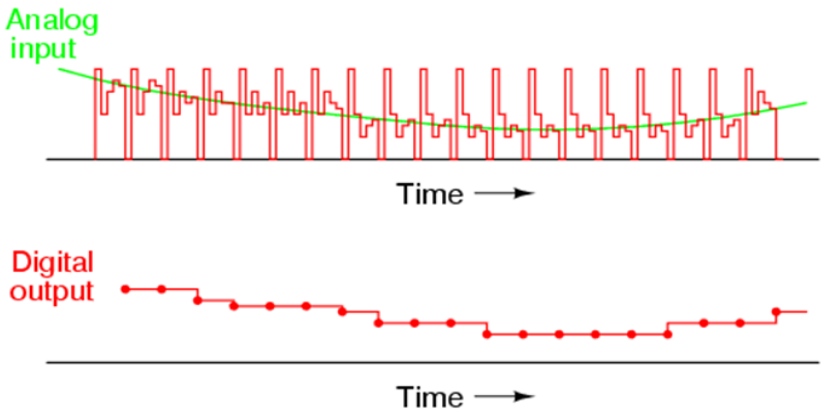
Successive approximation register analog-to-digital converters are common for low power A/D-conversion. This makes them suitable for wireless systems where power consumption limits operation time [6]. The SAR architecture mainly uses the binary search algorithm. The SAR ADC consists of fewer blocks such as one comparator, one DAC and one control logic. The main advantage of SAR ADC is good ratio of speed to power. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. The physical limitation of SAR ADC is it has one comparator throughout the entire conversation process. If

there is any offset error in the comparator, it will reflect on the all conversion bits so you must have a suitable comparator [7].

One method of addressing the digital ramp ADC's shortcomings is the so-called successive-approximation ADC. The only change in this design is a very special counter circuit known as a successive-approximation register. Here the register Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit. Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly. The circuit, and the outputs are shown in FIGURE4-a, and FIGURE4-b.



(a)



(b)

FIGURE4: a- SAR ADC circuit. b- The operation of SAR ADC

It should be noted that the SAR is generally capable of outputting the binary number in serial (one bit at a time) format, thus eliminating the need for a shift register. From FIGURE 4-b, it can be noted how the updates for this ADC occur at regular intervals, unlike the digital ramp ADC circuit [5].

3. proposed Moore SAR Logic circuit

In general, sequential circuits can be classified into two types: (1) those in which the output or outputs depend only on the present internal state (called Moore circuits) so the outputs can be taken directly from the output of flip flops (y= Q), and (2) those in which the output or outputs depend on both the present state and the input or inputs (called Mealy circuits) [8,9,10].

In this work the SAR is designed by using Moore sequential circuit and implemented by J-K Flip Flop for the first time, and since the SAR operation can be represented in the tree as seen in FIGURE5, then the state diagram can be shown in FIGURE 6. Here Em represents the Analog desire voltage which wanted to be digitize, and ea represents the voltage after DAC.

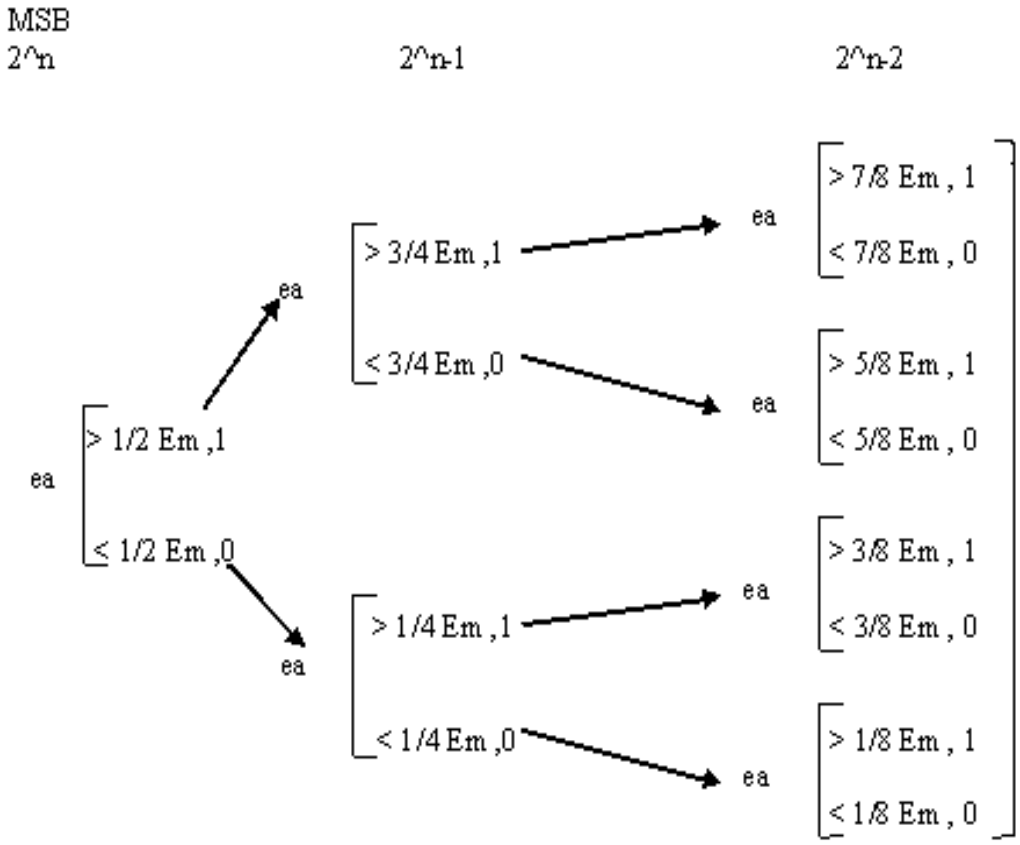


FIGURE 5: The operation of SAR

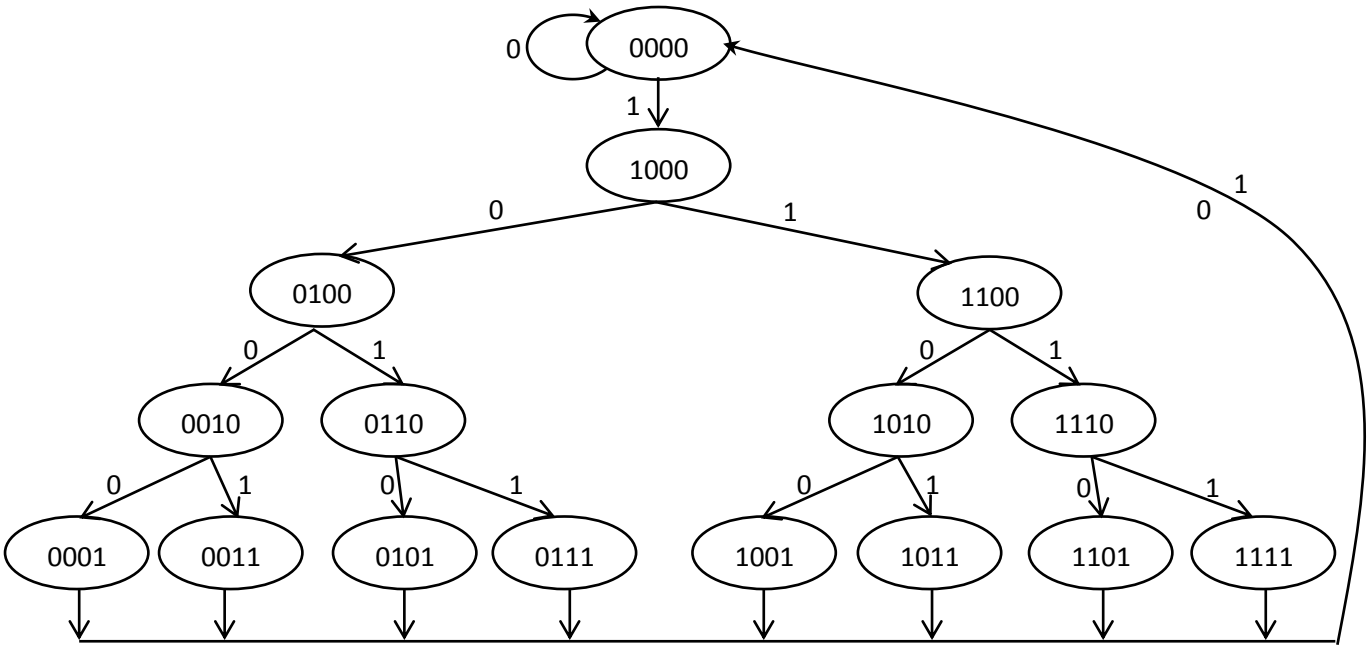


FIGURE 6: The state diagram of Moore SAR .

Then the state table can be shown in TABLE 1, and the J-K excitation table can be shown in TABLE 2.

previous State				Next State	
y4	y3	y2	y1	X= 0	X= 1
0	0	0	0	0000	1000
1	0	0	0	0100	1100
1	1	0	0	1010	1110
0	1	0	0	0010	0110
1	1	1	0	1101	1111
1	0	1	0	1001	1011
0	1	1	0	0101	0111
0	0	1	0	0001	0011
0	0	0	1	0000	0000
0	0	1	1	0000	0000
0	1	0	1	0000	0000
0	1	1	1	0000	0000
1	0	0	1	0000	0000
1	0	1	1	0000	0000
1	1	0	1	0000	0000
1	1	1	1	0000	0000

TABLE 1: State table

Input (X= 0)				Input (X= 1)			
J_4K_4	J_3K_3	J_2K_2	J_1K_1	J_4K_4	J_3K_3	J_2K_2	J_1K_1
0x	0x	0x	0x	1x	0x	0x	0x
x1	1x	0x	0x	x0	1x	0x	0x
x0	x1	1x	0x	x0	x0	1x	0x
0x	x1	1x	0x	0x	x0	1x	0x
x0	x0	x1	1x	x0	x0	x0	1x
x0	0x	x1	1x	x0	0x	x0	1x
0x	x0	x1	1x	0x	x0	x0	1x
0x	0x	x1	1x	0x	0x	x0	1x
0x	0x	0x	x1	0x	0x	0x	x1
0x	0x	x1	x1	0x	0x	x1	x1
0x	x1	0x	x1	0x	x1	0x	x1
0x	x1	x1	x1	0x	x1	x1	x1
x1	0x	0x	x1	x1	0x	0x	x1
x1	0x	x1	x1	x1	0x	x1	x1
x1	x1	0x	x1	x1	x1	0x	x1
x1	x1	x1	x1	x1	x1	x1	x1

TABLE 2: J-K excitation table

For simplification you can use a five bit Karnaugh Map as shown in TABLE 3 where the output of J_1 is determined.

y4y3 \ y2y1X	000	001	011	010	110	111	101	100
00			x	x	x	x	1	1
01			x	x	x	x	1	1
11			x	x	x	x	1	1
10			x	x	x	x	1	1

TABLE 3: Karnaugh map of J1

From TABLE 3, it can be seen that J_1= y3, and so on for all J-k's in all Flip-Flops. So the SAR J-K Flip-Flop hole circuit can be shown in FIGURE 8-a, and its block in FIGURE 8-b, here y1 represent the LSB, and y4 represent the MSB.

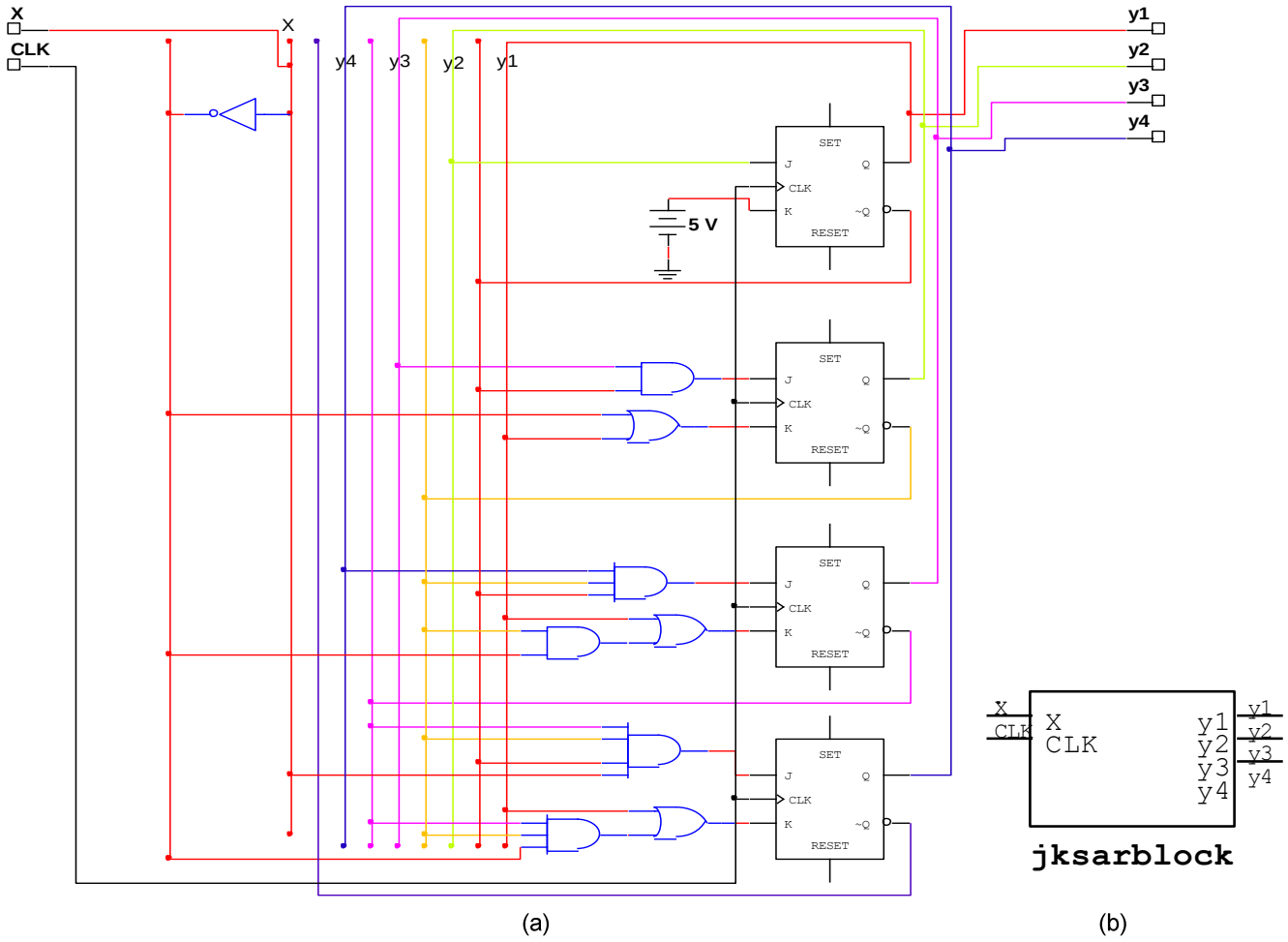


FIGURE 8: a- SAR J-K Flip-Flop. b- Blok of it.

4. Digital To Analog Circuit

The circuit of DAC is shown in FIGURE 9-a with its Block in 9-b, this type is called R/2R (Ladder) DAC which uses fewer unique resistor values. In this work, 5 v is taken as reference voltage, so that $(0000)_2$= 0 v, and $(1111)_2$= 5 v. The step size and output voltage are seen in equation (1), and (2), and since n= 4, then the step voltage (Vs) is 0.3125 v. The output voltage for $(1111)_2$ is equal to 4.6785 v, and by using TTL Logic circuit then VD= 5 v. Here R= 1kΩ, and Ref is equal to 1kΩ (from equation (2)).

$$V_s = V_{ref}/2^n \quad \ldots(1)$$

$$V_o = \frac{Ref}{R} VD\left(\frac{Do}{16} + \frac{D1}{8} + \frac{D2}{4} + \frac{D3}{2}\right) \quad \ldots(2)$$

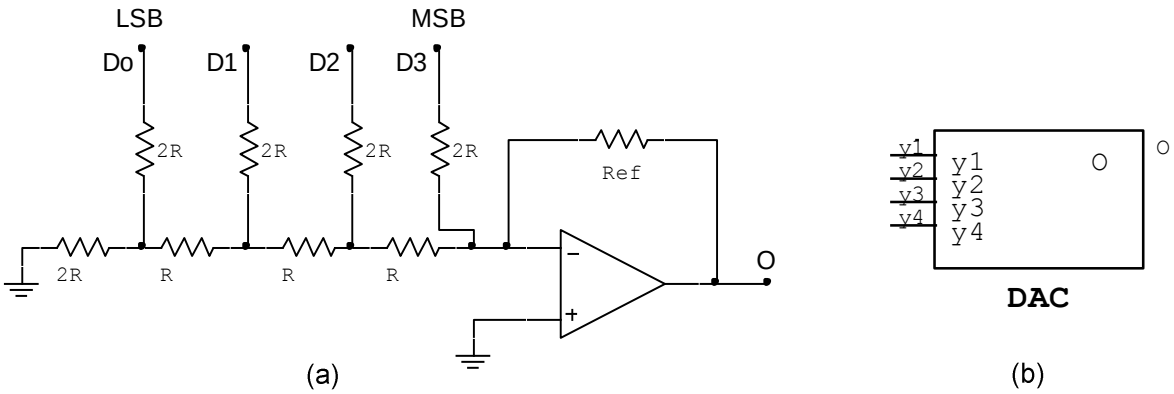


FIGURE 9: a-The circuit of DAC. b- The Block of DAC

5. Comparator

The 741 operational amplifier was used to compare the pervious state of ADC with the input signal . If the input signal is more than pervious state of ADC the OP-Amp give logic-1 ,else; give logic-0.

6. Clock

The 555 multivibrator was used to provide a clock to the circuit as shown in FIGURE (10). Here the two resistance are equal to each other in order to make the duty cycle equal to 50%.

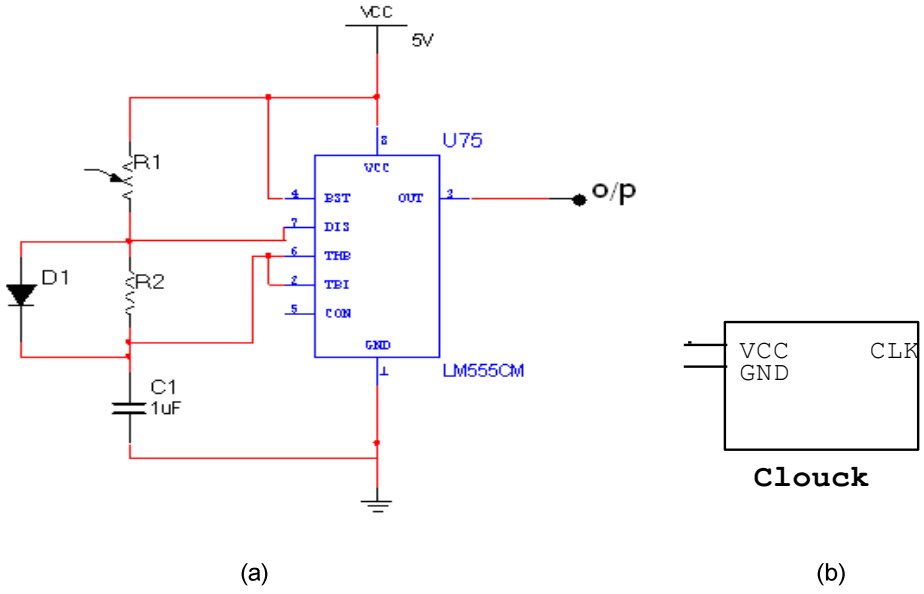


FIGURE 10: a- Block of Clock. b-CLK circuit

7. JK-Counter

In order to view the final result ; the mod-5, D-counter was designed and give the result throw logic circuit as a clock to the latch as shown in FIGURE 11-a, and its block in FIGURE 11-b.

8. Latch

The circuit of parallel in parallel out latch is used as shown in FIGURE (11-c) and its block is shown in FIGURE (11-d).

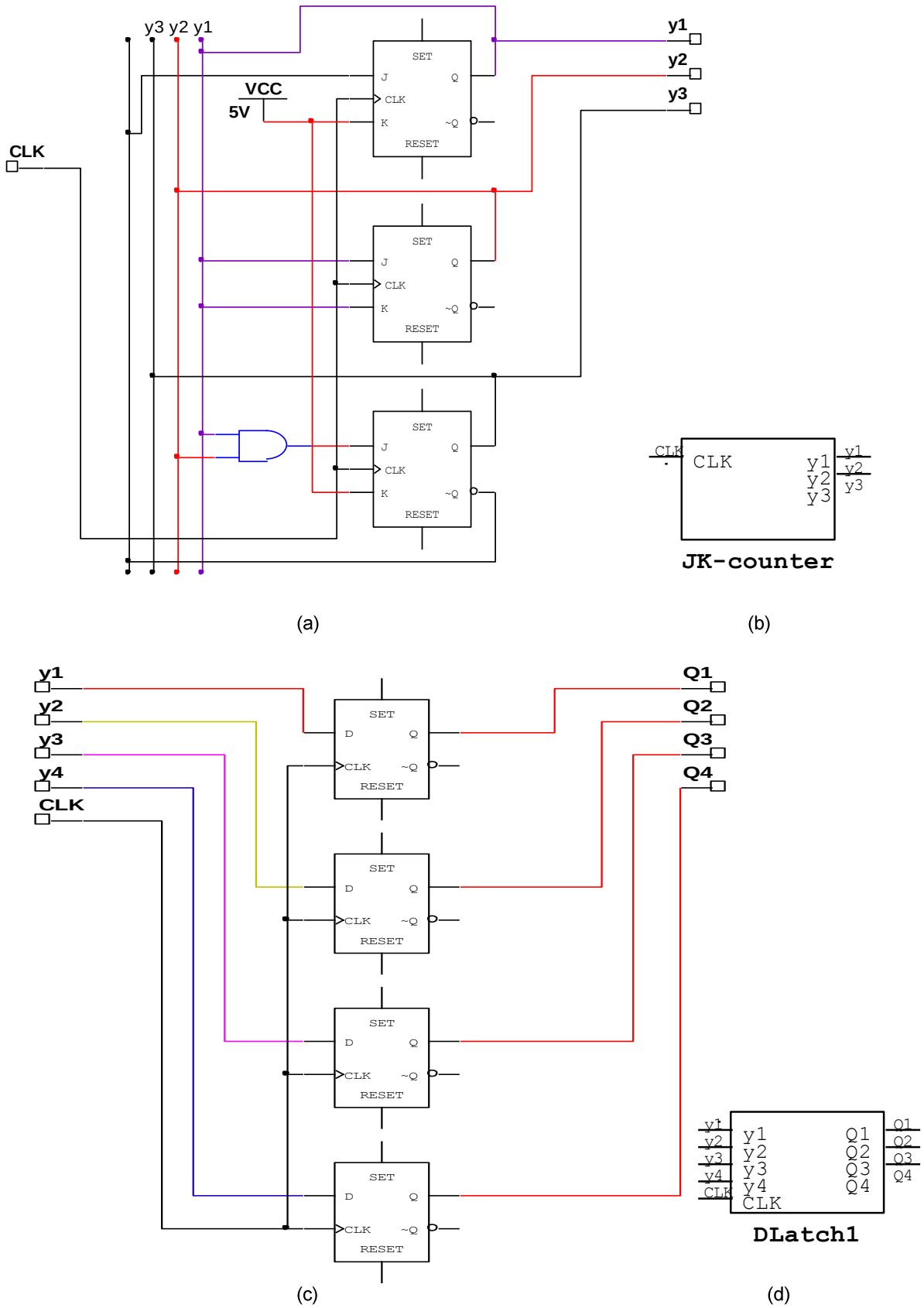


FIGURE 11: a- Jk counter. b- the block of it. c- D-Latch. d- The block of it.

9. Proposed Moore SAR ADC

The Hole circuit is shown in FIGURE 12. The circuit was tested first by DC input voltage, and second by AC input voltage with different voltages (under the range from 0-5 v). Here the results are obtained from Oscilloscope, DCD HEX display, and 4 props.

10. Results and Discussion

First Vref is set to DC voltage Like (3 v) for example as seen in FIGURE13, and the results is seen in FIGURE14.

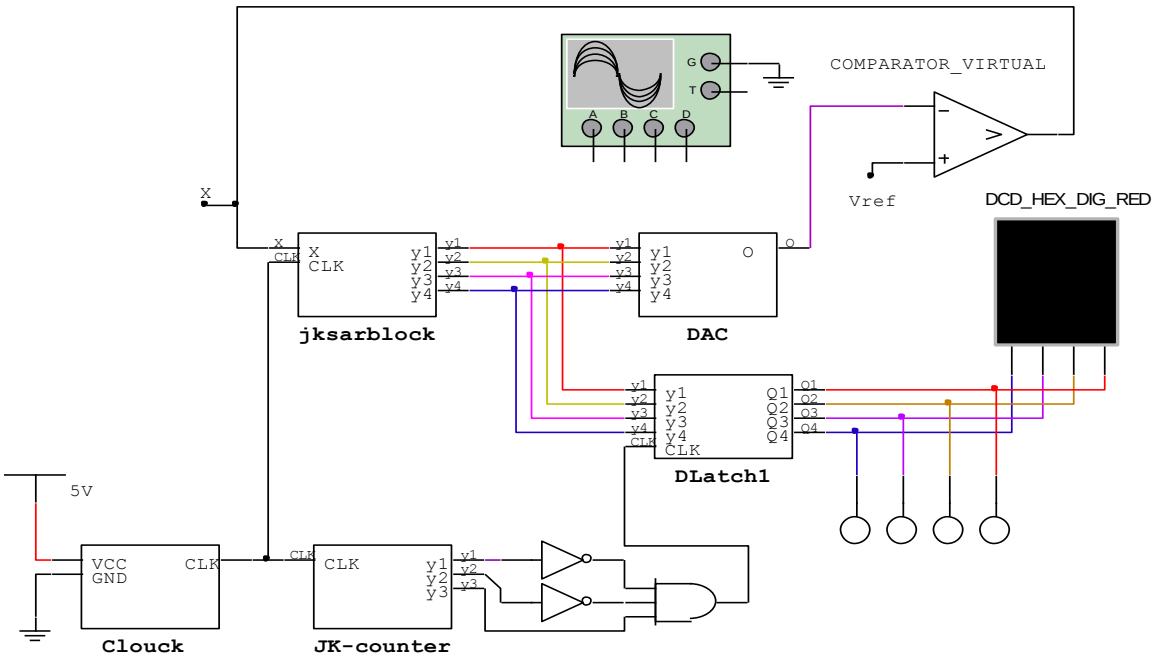


FIGURE 12: Moore SAR ADC circuit

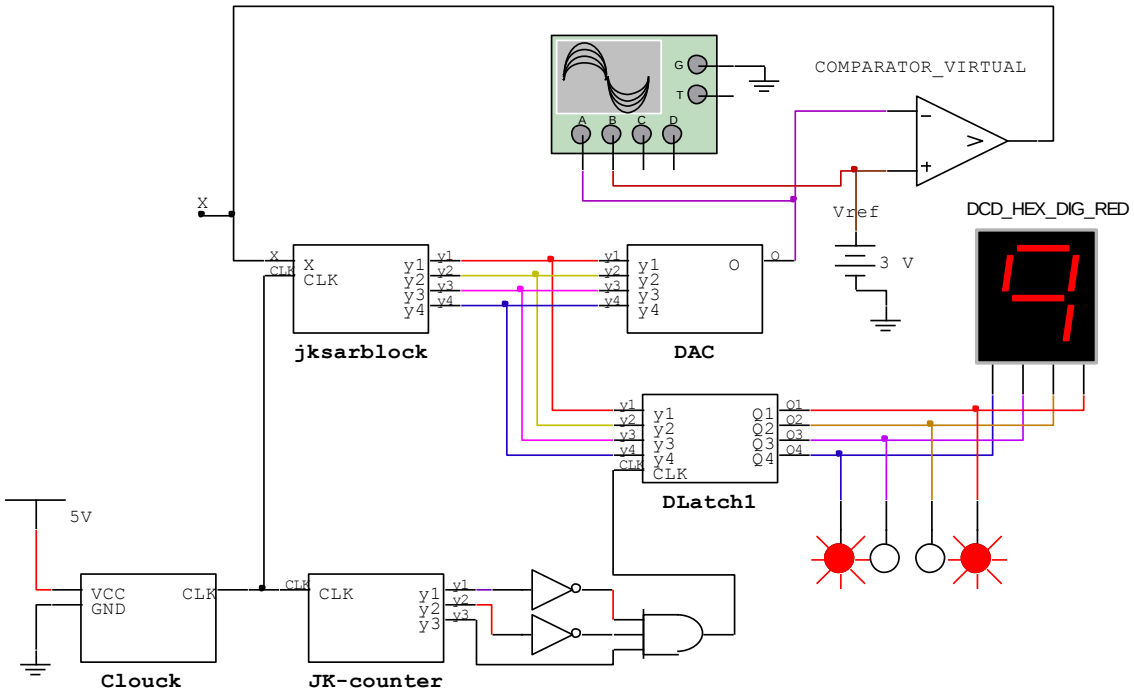


FIGURE 13: DC input voltage to the proposed circuit

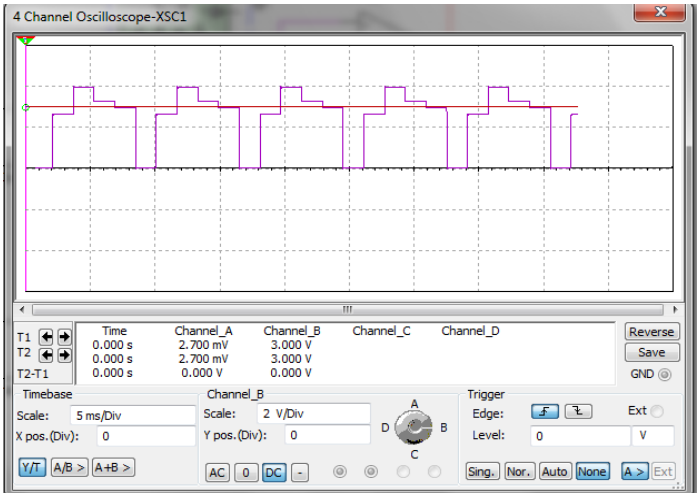


FIGURE 14: response to 3 v input.

You can see from FIGURE 13 that the result from BCD HEX display is (9) which is true since (9*0.3125= 2.8125) so the proposed circuit is indeed work successfully, also from FIGURE 14 it can be shown that the circuit track the input voltage until it reaches to it which exactly satisfy the idea of SAR. Finally the probe response is (1001) which equals to 9 in decimal.

Another tests are done by taking Vref equal to 1.5 v, and 5v, and the results are shown in FIGURE15 and FIGURE 16 respectively.

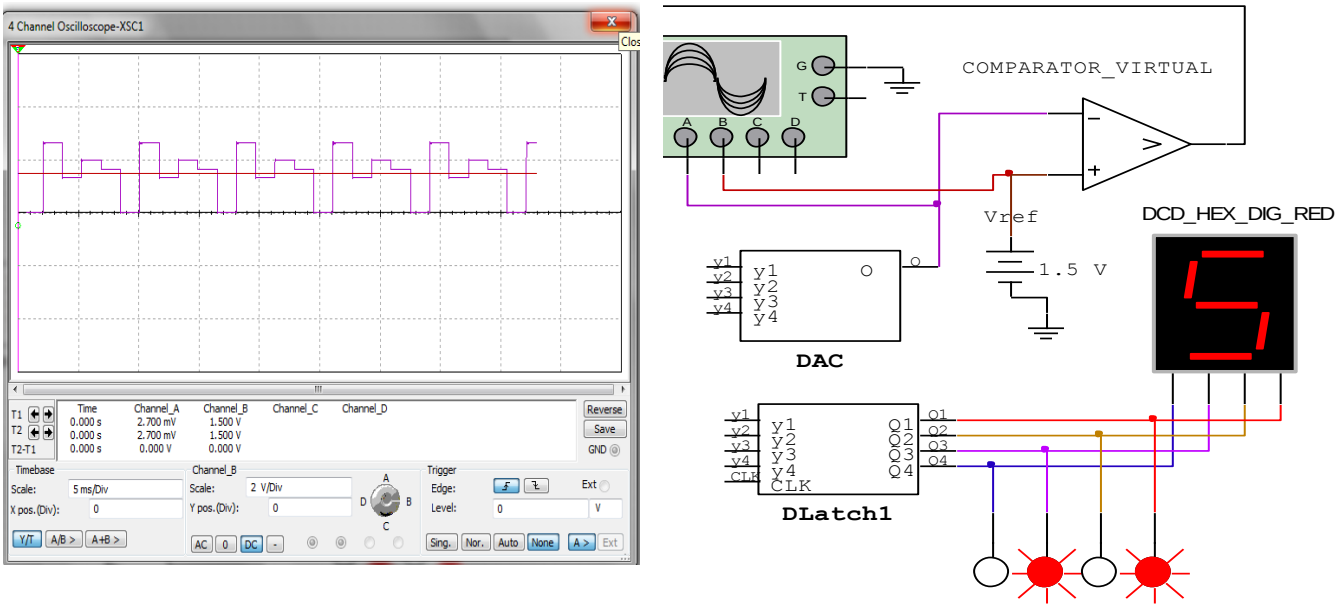


FIGURE 15: the results when Vref= 1.5 v

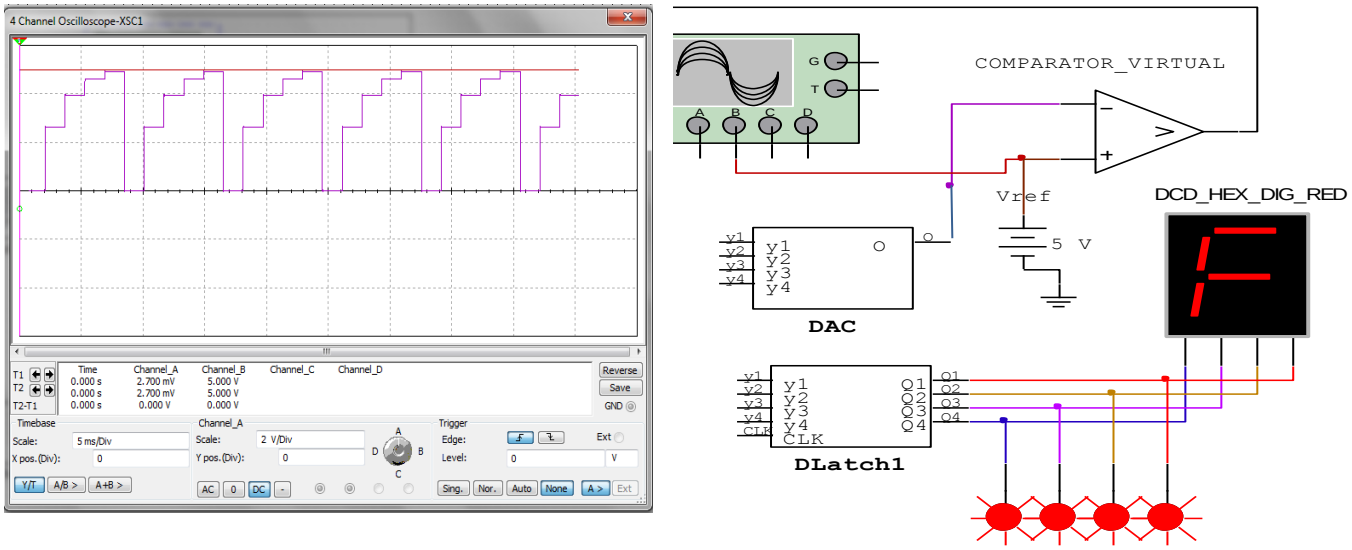


FIGURE 16: the results when Vref= 5 v.

Second test is done by setting Vref to AC voltage like for example Vref= 5sinwt, and the result is shown in FIGURE 17.Offcourse the results seen from the BCD HEX display and the probe are variable with time since Vref is variable. You can see from the reading of OSC. That the output of the proposed circuit is tracking the AC input until it reaches the value of it.

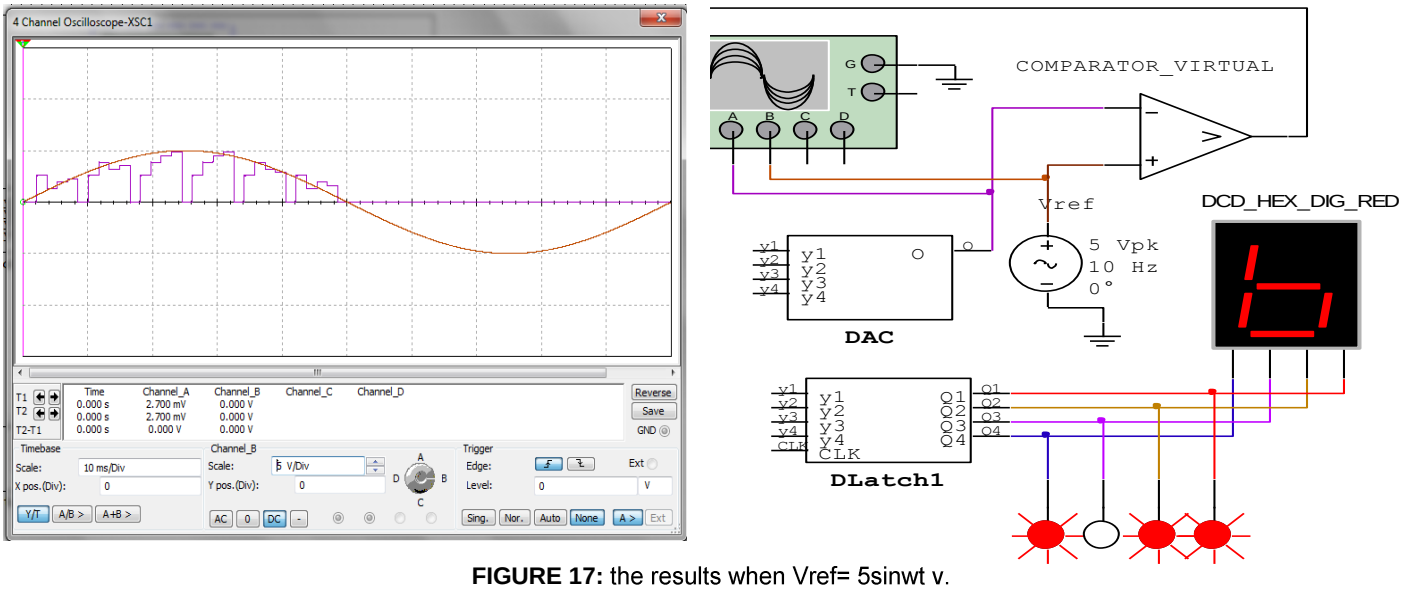


FIGURE 17: the results when Vref= 5sinwt v.

In this work the algorithm is designed with a low consumption power which is 11 m watt from 5 v supply voltage, with a clock frequency up to 8 MHz, and as compared with B. Ginsburg [4] which design an ADC with a 30 m watt of power and also 4 bit resolution, it can be seen that the proposed circuit consume low power, also J. Digel. [6] designs a circuit with 13 m watt consumption power but from 2.6 v source voltage with 6-7 bit and a rate up to 80 Ms/s, whereas the proposed design use 5 v supply voltage and consumes 11 m watt.S. Yan Ng[11] with his team design a 5 bits SAR with 600 MHz circuit and in spite of that it consumes a 30 m watt.

11. Conclusion

In this work a new approach is tested, which is design of Successive Approximation Register ADC with Moore Sequential Logic circuit, and simulated by using JK Flip-Flop with Multisim 11 program. It is found that the design was work successfully and easy to implement and you can digitize any input voltage (here from 0-5 v), offcourse you can increase the input voltage after redesign the DAC, but the step voltage will increase too so the accuracy will be decreased, so the solution is to design 5 or 6 bits SAR ADC where the step voltage will minimize. From the results it is found that the consumption power is 11 m watt with a clock rate up to 8 MHz so it consumes low power but with low bit accuracy, also the proposed circuit is worked with both DC and AC voltage, and it is very fast, accurate and implemented with a traditional logic gates like OR, AND, NOT, and JK Flip-Flop.

12. Future work

As a future work, increasing the bit accuracy from 4 bits to 6 or 7 bits, with high clock frequency and lowering the power consumption by for example using a capacitor array in the DAC circuit are taking into account.

13. REFERENCES

1. C. Cho. "A POWER OPTIMIZED PIPELINED ANALOG-TO-DIGITAL CONVERTER DESIGN IN DEEP SUB-MICRON CMOS TECHNOLOGY". PhD Thesis. Georgia Institute of Technology.2005.
2. K. Kval. "Design of an Analog to Digital Converter with Superior Accuracy/Bandwidth vs. Power Ratio". MSc Thesis. Norwegian University of Science and Technology Department of Electronics and Telecommunications. 2011.
3. T. Sundström. "Design of High-Speed Analog-to-Digital Converters using Low-Accuracy Components". Linköping University Department of Electrical Engineering. Linköping Studies in Science and Technology Dissertations. No. 1367. 2011.
4. B. Ginsburg. "Energy-Efficient Analog-to-Digital Conversion for Ultra-Wideband Radio". PhD Thesis. Massachusetts Institute of Technology Department of Electrical Engineering. 2007.
5. T. Kuphaldt. "Lessons In Electric Circuits". Volume IV-Digital, Fourth Edition. copy right Tony R. Kuphaldt. 2002.
6. J. Digel. and other. "A 6 bit and a 7 bit 80MS/s SAR ADC for an IR-UWB Receiver". Institute of Electrical and Optical Communications Engineering. University of Stuttgart. 2IHP. Frankfurt (Oder). Germany. 2011.
7. N. Barot. "Successive Approximation Analog to Digital Converter". Industrial Sponsor Srenik Mehta. Atheros Comm. 2010.
8. K. Breeding. Digital Design Fundamentals. Prentice Hall, Second Edition, 1992, pp 158-160.
9. E. Hwang. Digital Logic and Microprocessor Design With VHDL. La Sierra University. Books/cole, 2005, pp 202-214.
10. T. Floyd. DIGITAL FUNDAMENTALS. Prentice Hall Ninth Edition Pearson Education Interactional, 2006, pp 447-458.
11. S. Yan Ng. and other "A low-voltage CMOS 5-bit 600MHz 30mW SAR ADC for UWB wireless Receivers", Department of Electrical and Computer Engineering, The Ohio State University Columbus, 2005 IEEE, 187-190.