Dual-Diameter Variation –Immune CNFET-Based 7T SRAM Cell

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Abstract

This paper proposes a variation – tolerant dual-diameter CNFET-based 7T (seven transistor) SRAM (static random access memory) cell. The use of appropriate DCNT (diameter of CNFET) and hence Vt of CNFETs is a critical piece of our design strategy. In this work, dual-Vt and dual-diameter CNFETs have been used using suitable chiral vectors for appropriate transistors. It also investigates the impact of process, voltage and temperature variations on its design metrics and compares the results with its counterpart – CMOS-based 7T SRAM cell and standard 6T SRAM cell (only few parameters). The proposed SRAM cell offers 1.35× and 1.25× improvement in standby power on an average @ VDD = 1 V and 0.9 V respectively, 30% improvement in SNM (Static Noise Margin) over CMOS-based 7T cell. Proposed design outperforms 6T in terms of 71.4% improvement in RSNM and shows same read stability as its CMOS counterpart, It shows its robustness by offering 1.4× less spread in TRA (read access time) at 1 V and 1.2× less spread in TRA at 0.9 V than that of its CMOS counterpart at the expense of 1.6× read delay. The proposed bitcell also exhibits higher performance while writing (takes 1.3× and 1.2× less TWA (write access time) @ VDD = 1 V and VDD= 0.9 V respectively). It also proves its robustness against process variations by featuring tighter spread in TWA variability (1.4× and 1.2× @ VDD= 1 V and 0.9 V respectively).

Keywords: Carbon Nanotube Field Effect Transistor (CNFET), Chirality Vector, Cell Ratio, Pull-up Ratio, Static Random Access Memory.

1. INTRODUCTION

Due to increased power density and thermal stress, device parameter variability increases and hence PVT (process, voltage and temperature) variations are visible across a single die (within-die or WID, e.g., in the case of temperature or voltage variations) or across several dies (die-to-die or D2D, e.g., in the case of clock speed and leakage power variations). These fluctuations are more pronounced in minimum-geometry devices commonly used in area-constraint circuits such as SRAM (static random access memory) cells [1]. SRAM constitutes more than half of chip area and more than half of the number of transistors in modern designs [2]. Hence, the design and evaluation of SRAM cell in terms of its design criteria is not only important but also its robustness against PVT variations is essential in deep submicron technology such as 32 nm technology node.

This paper makes the following contribution. 1) In view of the ultra-low power requirement and variability issue, a dual-diameter CNFET-based 7T SRAM cell is proposed in this paper; its performance is assessed and compared with its CMOS counter part. 2) It has been demonstrated that the proposed design outperforms CMOS-based 6T SRAM cell in terms of static noise margin (SNM), read static noise margin (RSNM). 3) This paper has established that the proposed design offers better read stability, better write-ability and improved tolerance against PVT variation, which has been achieved by proper selection of chirality vector for appropriate transistor in the proposed design. 4) In standby mode SRAM cells are inactive and consume power for data retention due to various leakage components. This paper also has investigated leakage power consumed by proposed design and its CMOS counter part (CMOS-based 7T SRAM cell) and demonstrated that the proposed design offers improvement in data retention power.

The remainder of this paper is organized as follows. Basic characteristics of CNFET structure is introduced in Section 2. SRAM's design metrics, failure mechanisms, and operations are briefly reviewed in Section 3. Section 4 presents a brief discussion on CMOS-based 7T SRAM cell (hereafter called 7T) and CNFET-based 7T SRAM cell (hereafter called CNFET-7T). Simulation measurements and comparisons between proposed CNFET-7T and 7T are detailed in Section 5. Finally, the conclusion of the paper appears in Section 6.

2. CHARACTERISTICS OF CNFET STRUCTURE

Carbon nanotube (CNT) has been proposed as possible replacements for copper interconnect due to their large conductivity and current carrying capabilities in the literature [3]-[6]. CNTs are sheets of graphite rolled into hollow cylinders of diameters varying from 0.4 nm to 4 nm. Depending on the direction in which they are rolled (called chirality) a CNT can be semiconducting with distinct band gap or it can be metallic with no bandgap. The resulting structure is called single-walled carbon nanotube (SWCNT) [7] as shown in Fig. 1. If several SWCNTs with varying diameter are rolled concentrically inside one another, then the resulting structure is called multi-walled carbon nanotube (MWCNT), diameter ranging from several nm to tens of nm [8], as shown in Fig. 2. As variation is inherent to technology scaling, it is difficult to improve device performance by reducing the feature size of the devices beyond 65 nm technology node. Therefore, last few years witnessed a tremendous increase in nanotechnology research, especially the nanoelectronics. Various nanoelectronic technologies which have received researchers' attention in the last few years are single-electron transistor, nanotube, nanowire, molecular devices, etc. Carbon nanotubes (CNTs) are the most studied material of these new materials because of the unique electro-mechanical properties. Carbon nanotube field effect transistor (CNFET) using CNT is the most promising technology to extend or complement traditional CMOS technology due to: 1) similar operating principle and device structure and 2) the reusability of established CMOS design infrastructure. Above all, CNFET has the best experimentally demonstrated drive current. Moreover, with the use of CNFET technology, the historic trend of device scaling can be continued for another 2 to 3 technology generations and the CMOS technology roadmap can be extended up to 10 nm device length.

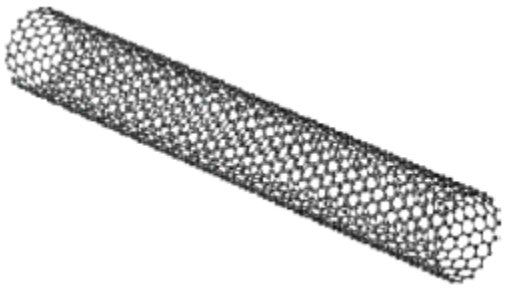

FIGURE 1. SWCNT.

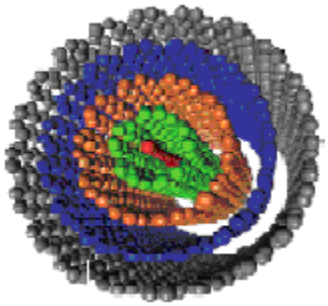

FIGURE 2. MWCNT.

Most of the fundamental limitations of traditional silicon MOSFETs are mitigated in CNFET. With ultralong (~1 μm) mean free path for elastic scattering, a ballistic or near-ballistic transport can be obtained with the use of CNT under low voltage bias to achieve the ultimate device performance [9]-[12]. Its quasi-1-D structure provides better electrostatic control over the channel region [13]. Ballistic transport operation and low I_{OFF} (OFF-current) make the CNFET a suitable device for high performance and increased integration.

The CNFETs can be scaled down to 10 nm channel length and 4 nm channel width, thereby enhancing throughput in terms of speed and power compared to MOSFET [14]. An SWCNT can work differently depending on its chirality (n1, n2) – the direction in which it is rolled up. The CNT acts as metal if n1 = n2 or n1 – n2 = 3i, where i is an integer. Otherwise, CNT works as semiconductor. The threshold voltage (Vt) of CNFET can be varied with CNT diameter (DCNT) as shown below. Vt of CNFET is approximated to the first order as the half band gap (Vt ≈ Eg/2q), which is an inverse function of diameter. The DCNT and Vt of CNT are calculated using chirality vector (n1, n2) and Vπ respectively as [14]

$$D_{CNT} = \frac{a}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \qquad (1)$$

$$V_t \approx \frac{E_g}{2q} = \frac{aV_\pi}{\sqrt{3} \times qD_{CNT}} \qquad (2)$$

where E_g is energy gap, q = electronic charge, a = √3d = 2.49 Å is the lattice constant (where d ≈ 1.44 Å is the inter–carbon–atom distance) and V_π = 3.033 eV is the carbon π–to–π bond energy in the tight bonding model. In this paper dual-V_t and dual-diameter CNFETs have been used using chrial vector values (11, 0) and (13, 0). The D_{CNT} of the CNFET with chiral vector value (11, 0) and (13, 0) are computed using (1) to be 0.8719 nm and 1.03 nm respectively. The V_t of the CNFET with chiral vector value of (11, 0) and (13, 0) are computed using (2) to be 0.5018 V and 0.4246 V respectively. Compared to silicon technology, the CNFET shows better device performance, even with device nonidealities. Compared to CMOS circuits, the CNFET circuits with one to ten CNTs per device is about two to ten times faster [15, [16]. A typical structure of a CNFET is illustrated in Fig. 3. CNTs are placed on substrate having dielectric constant of Ksub = 4. The tubes are separated by a high-k (Hi-k) material called hafnium (HfO2) having dielectric constant of (Kox) 16 and thickness (tox) of 4 nm. The effective width of the multi-tube CNFET (Wg) is defined as Wg = Pitch×(NCNT)+DCNT, where Pitch is the distance between centre of two adjacent tubes, NCNT is the number of tubes and DCNT is the diameter of tube. Default value of gate width (Wg = 6.4 nm) has been used for all the CNFETs used in this paper because single tube has been used for all the CNFETs. Other important device and technology parameters related to CNFET are tabulated in Table 1. The I-V characteristics of used CNFETs with chirality vector (11, 0) and (13, 0) and NMOS with zero bias threshold voltage, Vtn0 = 0.63 V are plotted in Fig. 4. P-type CNFET used in the proposed design has I-V characteristics with opposite polarity (not shown).

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
Wg	The width of metal gate (sub_pitch)	6.4 nm
Ldd/Lss	Length of doped CNT drain-side/source-side extension region	32 nm
t_{ox}	The thickness of high-k top gate dielectric material (planer gate).	4 nm
K_{ox}	Dielectric constant of high-K gate oxide	16
(n_1, n_2)	Chirality of the tube	(11, 0) , (13, 0)
Vfbn	Flat band voltage for N-CNFET	0 eV
Lgef	The mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering (Lceff).	200 nm
n_CNT	Number of tube	1

TABLE 1. Device and Technology Parameters for CNFET.

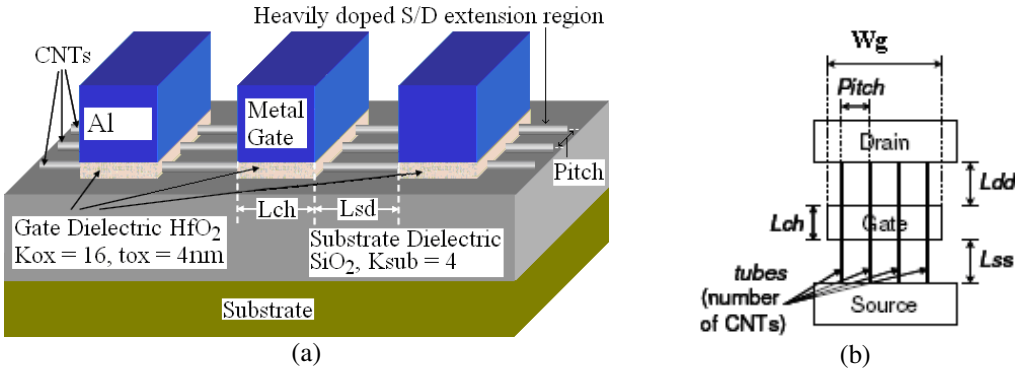

FIGURE 3. (a) A Typical CNFET Structure with Multiple Channels, High-*k* Gate Dielectric Material. The Channel Region of CNTs is Un-doped, and the Other Regions of CNTs are Heavily Doped. (b) Defines Parameters Such as Wg, Pitch, Ldd, Lss, Lch [14]-[16].

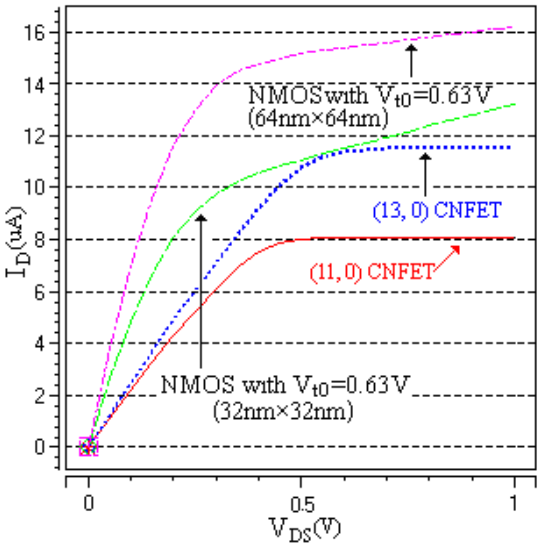

FIGURE 4. I-V Characteristics of NMOS and CNFET.

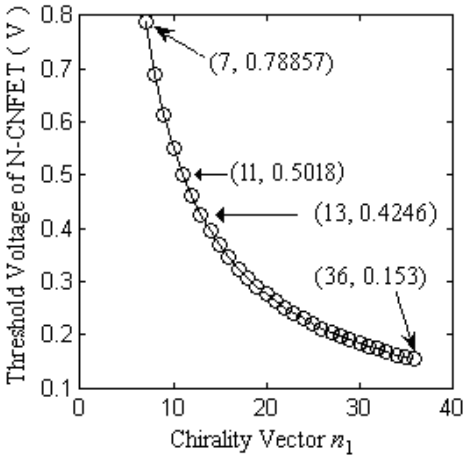

FIGURE 5. V_t Versus Chirality Vector (n_1).

The threshold voltages of N-CNFET have been computed using (1) and (2) with chirality vector ranging from (7, 0) to (36, 0). First, the D_{CNT} has been calculated substituting the value of the constant π = 3.142, the value of the lattice constant a = 2.49 Å and the value of n_1 ranging from 7 to 36 keeping n_2 = 0. Next, the threshold voltage V_t is calculated substituting the value of a = 2.49 Å, the value of the carbon π–to–π bond energy V_π = 3.033 eV, the value of electronic charge q = 1.6×10^{-19} C and the computed value of D_{CNT}. The computed values of threshold voltage for each values of n_1 ranging from 7 to 36 are plotted in Fig. 5. The plot in Fig. 5 shows two end points with V_t = 0.78857 V at n_1 = 7 and V_t = 0.153 V at n_1 = 36. Other two important points in this plot are (11, 0.5018) and (13, 0.4246) which indicates V_t = 0.5018 V at n_1 = 11 and V_t = 0.4246 V at n_1 = 13. These are the threshold voltage of CNFETs used in the proposed design. The threshold voltage (V_t) of P-type CNFET employed in this design has an opposite polarity (not shown).

3. SRAM DESIGN METRICS, FAILURE MECHANISMS AND OPERATIONS

3.1. SRAM Design Metrics

Design of SRAM requires the smallest transistors, which are particularly sensitive to process variations. Balancing the trade-offs between small areas, low powers, fast reads/writes are an

essential part of any SRAM design. That is, SRAM design requires balancing among various design criteria such as minimizing cell area using smaller transistor, maintaining read/write stability, minimizing power consumption by reducing power supply, minimizing read/write access time, minimizing leakage current, reducing bitline swing to reduce power consumption, improving soft error immunity, etc. Some of the design criteria are conflicting in nature. For example, higher cell ratio (CR) prevents read failure, but results in larger cell area, increased leakage and decreased write-ability.

3.2. Failure Mechanism of SRAM Cells

Failures in SRAM cell may be of three types – hard failures, soft failures and parametric failures. 1) *Hard failures* are caused by open or short. 2) *Soft failures* – there are major three sources of soft failures. They are alpha particles released from the radioactive impurities such as packaging materials, high energy neutrons from terrestrial cosmic radiations and the interaction of cosmic ray thermal neutron. 3) *Parametric failures* – since these failures are caused by the variations in the device parameters, these are known as the parametric failures. Parametric failures include access failure defined as unacceptable increase in access time; read failure is defined as flipping of cell content while reading; write failure is defined as inability to write to a cell and hold failure is defined as flipping of the cell state in the standby mode, especially when V_{DD} approaches or falls below DRV (data retention voltage) [17].

3.3. SRAM's Modes of Operations

An SRAM cell offers the following basic modes of operation: 1) *Data retention or standby mode* – an SRAM cell is able to retain the data indefinitely as long as it is powered. 2) *Read operation* – an SRAM cell is able to communicate its stored data. This operation does not affect the data i.e., read operation is non-destructive unlike read operation of DRAM cell. 3) *Write operation* – the data of an SRAM cell can be set to any binary value regardless of its original stored value.

4. CMOS-BASED 7T SRAM CELL AND PROPOSED CNFET-BASED 7T SRAM CELL

4.1. CMOS-Based 7T SRAM Cell

Authors in [18] proposed a 7T cell similar to the proposed CNFET-7T shown in Fig. 6 to reduce the activity factor αBL for reduction of dynamic power while writing to a cell given by PWRITE = αBL×CBL×V2×FWRITE. But static power consumption in a SRAM cell is more critical than dynamic power consumption since dynamic power is consumed only during read/write operation due to bitline charging and discharging and whole part of the cache remains idle most of the time except the row being read from or written to. Therefore, this paper has proposed a CNFET-7T and demonstrated that the proposed design is better in terms of static (hold) power and write power. In addition to that, 7T's transistor sizing constraint for meeting its functionality poses additional area penalty.

Read/Write operation: both BL (bitline) and BLB (bitline bar) are precharged high before and after each read/write operation. The write operation in 7T cell starts by turning MN5 off. Complement of data to be written to node Q is applied to BLB and MN3 is turned on by asserting WL high, leaving MN4 off. BL and MN4 do not take part in write operation. To write a "0" at Q, BLB is made high which writes "0" at Q, which in turn drives INV1 to store a "1" at QB. To write a "1" at Q, BLB is made low, which discharges Q2 (stored value at QB) thereby flipping Q to "1" which in turn drives INV1 to store a "0" at QB. Writing is completed after two inverters delay. During standby mode MN3 and MN4 are kept off applying WL and R low, MN5 is kept on asserting W high. Read operation of 7T cell is similar to that of 6T cell. BLB discharges through the critical read path consists of MN3, MN5 and MN1 during read operation with QB storing "0". BL discharges through the read path MN4 and MN2 during read operation with QB storing "1".

Important device and technology parameters for the 6T and 7T cell are tabulated in Table 2. As MN1 ≥ 3 and MN2 ≥ 2 ensure stable read operation, the transistors in 7T cell are sized as shown in the Table 2. The 7T also requires low-Vt MN5. To avoid extra masking cost and to fulfill this requirement, the diameter of MN5 is increased to reduce its V_t in proposed design. Other transistors used for the design are of minimum-sized to keep smaller cell size.

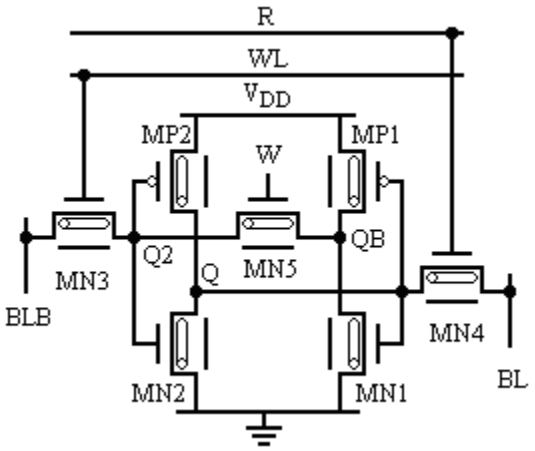

FIGURE 6. Proposed CNFET-Based 7T SRAM Cell.

Parameter	CMOS-based 6T	CMOS-based 7T
V_{tn0}	0.63 V	0.63 V
V_{tp0}	-0.5808 V	-0.5808 V
MP1, MP2	W = 32 nm, L = 32 nm	W = 32 nm, L = 32 nm
MN1	W = 64 nm, L = 64 nm	W = 96 nm, L = 32 nm
MN2	W = 32 nm, L = 32 nm	W = 64 nm, L = 32 nm
MN3, MN4	W = 32 nm, L = 32 nm	W = 32 nm, L = 32 nm
MN5	–	W = 32 nm, L = 32 nm

TABLE 2. Device and Technology Parameters of 6T and 7T.

4.2. Proposed CNFET-Based 7T SRAM Cell

CNFET-based designs have some fabrication issues, which are likely to be overcome shortly. CNFET-based circuit with small width CNFET suffers from CNT-specific imperfections such as 1) CNT diameter variations, 2) CNT density (count) variations, 3) Mis-positioned CNTs and 4) presence of m-CNTs (metallic CNTs). Most of the fabrication issues like positioning and alignment of CNTs along with the presence of metallic CNTs have been solved [19]-[32]. Moreover, CNFET can be fabricated using the existing Si-CMOS infrastructure and it can also be integrated with Si-CMOS on the same chip [33]. Therefore, this work has implemented CMOS-based 7T SRAM cell using dual-diameter CNFETs as shown in Fig. 6. To investigate the performance in terms of various design metrics, extensive simulations are run on HSPICE and finally CNFETs with two different diameters are selected to achieve optimum results. As mentioned in Section 2, the diameter selected for MN3 and MN5 is 1.03 nm to make it more conductive as the drive current through CNT is proportional to its diameter. The diameter of other five transistors is selected to be 0.8719 nm. The values of device diameters, threshold voltages and the corresponding chirality vectors are tabulated in Table 3. As mentioned in Section 2, single-tube CNFETs are used. The diameter used for MN3 and MN5 is 1.03 nm and for other transistors is 0.8719 nm.

CNFETs	Chirality vector	Threshold Voltage (V)	Diameter (nm)
MP1, MP2, MN1, MN2, MN4	(11, 0)	|0.5018|	0.8719
MN3	(13, 0)	0.4246	1.03
MN5	(13, 0)	0.4246	1.03

TABLE 3. Device Parameters of Proposed Design.

5. SIMULATION MEASUREMENTS AND COMPARISONS

This Section presents measurements of various design metrics which are measured during simulation on HSPICE using the experimentally validated CNFET model [14]–[16] and the 32 nm CMOS Berkeley Predictive Technology Model (BPTM) [34]. The CNFET model has been calibrated to 90% accuracy with experimental data (ac and dc characteristics) from fabricated CNFET circuits [35]. Monte Carlo simulations are performed for the measurements. Monte Carlo simulation is a method for iteratively evaluating a design. The goal is to determine how random variation on process parameters, voltage and temperature affects the performance and reliability of a design. The arithmetic mean (μ) is the measure of central tendency that is found to fluctuate less than any other measure of central tendency if many samples are drawn from the same statistical data and standard deviation (σ) is a measure of dispersion (or variability) that states numerically the extent to which individual observations vary on the average.

5.1. Data Retention or Hold Power

The leakage current is the major contributor to the power consumption in the SRAM cell. The total leakage current in an SRAM cell mainly consists of the subthreshold leakage current (I_{sub}), the gate leakage current (I_{gate}) and the reverse-biased drain- and source-substrate junction band-to-band tunneling (BTBT) leakage current (Ijn) through different transistors as shown in Fig. 7 [36].

$$I_{sub} = I_{sub\,MN4} + I_{sub\,MN1} + I_{sub\,MP2}$$
$$I_{jn} = 2I_{jn\,MN3} + I_{jn\,MN4} + I_{jn\,MN1} + I_{jn\,MP2} + 2I_{jnMN5}$$
$$I_{gate} = I_{gd\,MN3} + I_{gs\,MN3} + I_{gd\,MN4} + I_{gd\,MP2} + I_{gd\,MN2} + I_{gs\,MN2} + I_{gd\,MP1} + I_{gs\,MP1} + I_{gd\,MN1}$$
$$I_{leak} = I_{sub} + I_{jn} + I_{gate} \quad (3)$$

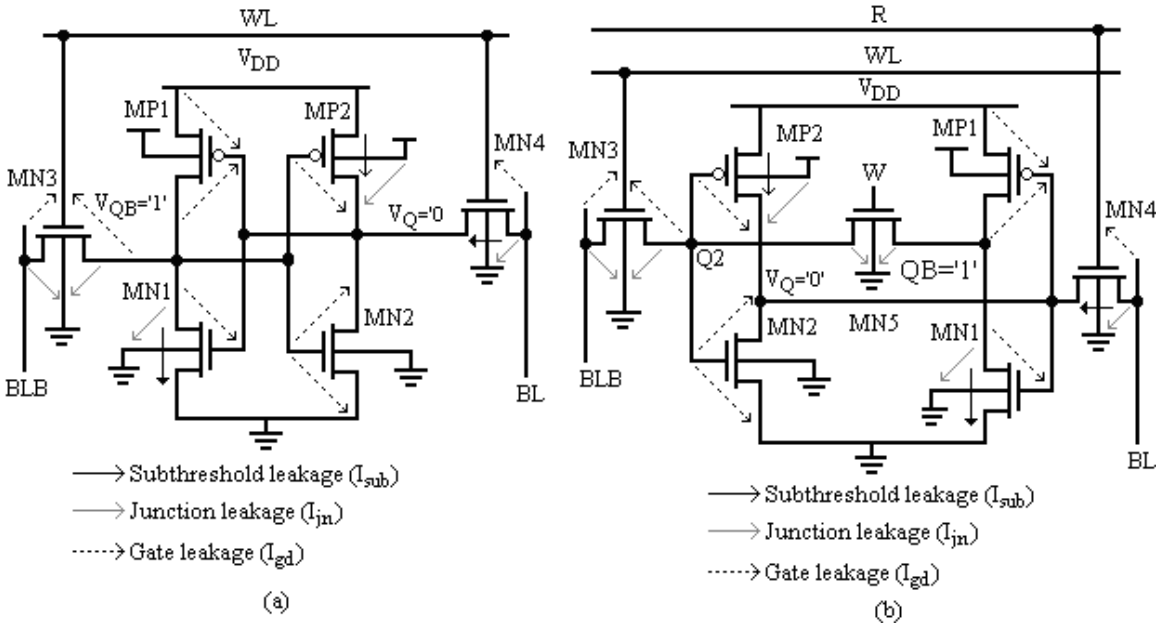

FIGURE 7. Leakage Components in (a) Standard 6T SRAM Cell (b) CNFET-7T SRAM Cell.

Fig. 7 shows the various leakage components in a standard 6T cell and CNFET-7T SRAM cell. Equation (3) is applicable to CNFET-7T SRAM cell or 7T (Fig. 7(b)). Total leakage current Ileak is dependent on stored value, device count, and device size. The leakage power (HPWR) (variously known as data retention power or hold power) consumed due to these leakage currents is measured at nominal voltage of VDD = 1 V and at 0.9 V (–10% of VDD) for 7T and CNFET- 7T. The measured results are reported in Table 4. The normalized values of H_{PWR} with QB storing "1"

and “0” are presented in bracket and plotted in Fig. 8 and 9 respectively for making the comparison easier. As can be observed from the Table 4, 7T consumes 1.5× and 1.4× higher hold power than that of proposed CNFET-7T at VDD = 1 V and at VDD = 0.9 V with QB storing “1” respectively. It also shows that 7T consumes 1.2× and 1.1× higher hold power than that of proposed CNFET-7T at VDD = 1 V and at VDD = 0.9 V with QB storing “1” respectively. Thus CNFET-7T offers 1.35× and 1.25× improvement in HPWR on an average @ VDD = 1 V and 0.9 V respectively. This is attributed to the extra cell area of 7T. It is evident from (3) that, leakage current obviously increase with cell area, since all the components of Ileak are dependent on transistor sizes. Moreover, OFF-current of CNFET is much lower than that of MOSFET.

SRAM	Hold Power with QB storing “1” (pW)	Hold Power with QB storing “0” (pW)	V_{DD} (V)
CMOS-base 7T	222.9(1.5)	69.3(1.2)	1
CNFET-based 7T	148.6(1)	57.73(1)	1
CMOS-base 7T	133.7(1.4)	51.8(1.1)	0.9
CNFET-based 7T	95.5(1)	47.11(1)	0.9

TABLE 4. Hold Power (H_{PWR}).

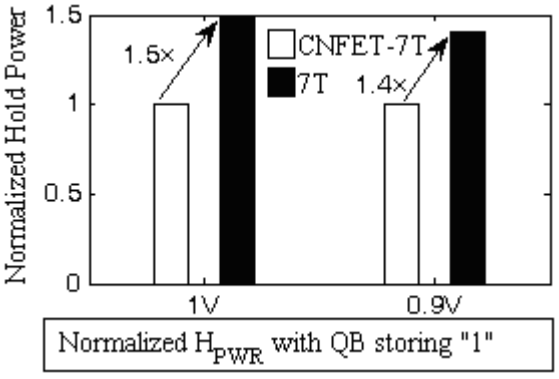

FIGURE 8. Normalized H_{PWR} with QB storing “1”.

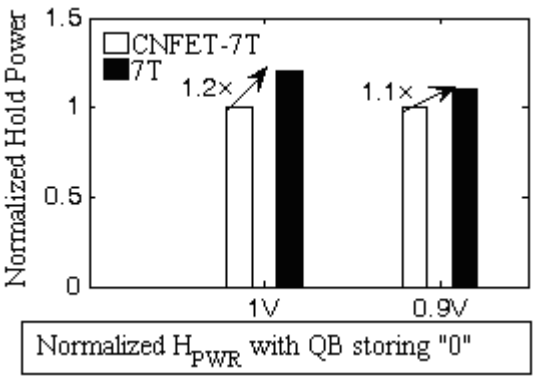

FIGURE 9. Normalized H_{PWR} with QB storing “0”.

5.2. Static Noise Margin Measurements

The static nose margin (i.e. SNM or hold SNM) of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. SNM of an SRAM is a widely-used design metric that measures the cell stability. Fig. 10 shows a conceptual test setup for measuring SNM of 6T (The similar set up is used for measuring SNM of 7T and CNFET-7T). The measured results are plotted to obtain "butterfly curve". Fig. 11 plots “butterfly curve” of 6T. The butterfly curve is obtained in the following way with the test circuit: 1) Word line (WL) is biased at ground and bit-lines (BL, BLB) are biased at supply voltage. 2) Voltage of N1 is swept from 0 V to supply voltage while measuring voltage of QB. 3) Voltage of N2 is swept from 0 V to supply voltage while measuring voltage of Q in the same way. 4) Measured voltages are plotted to obtain a butterfly curve. The side length of maximum-sized square that can be fitted within the smaller wing of the butterfly curve represents the SNM of the cell. This definition holds good because, when the value of noise voltage (VN1 or VN2) increases from 0, the VTC (voltage transfer characteristic) for INV1 (inverter 1) formed with MP1 and MN1 moves to the right and the VTC–1 (inverse VTC) for INV2 (inverter 2) formed with MP2 and MN2 (Fig. 10) moves downward. Once they both move by the SNM value, the curves meet at only two points and any further noise flips the cell [37]. As can be seen in the plot, initially node QB remains stable, but as the noise source at node Q increases, QB starts falling, eventually flipping the cell. Fig. 12 shows the comparison among 6T, 7T and CNFET-7T in terms of SNM in a single plot for making the comparison easier. As observed from Fig. 12, the SNM of 6T cell is 165 mV where as the SNM of 7T is 250 mV and that of CNFET-7T is 325 mV, showing 51.5% improvement in 7T and 97% improvement in CNFET-7T over 6T.

Compared to 7T, the proposed CNFET-7T offers 30% improvement in SNM. To understand why this has happened, remember that, both the Inverters of 7T are LO-skewed having $\beta_p/\beta_n < 1$ because of stronger NMOS drivers (MN1 = 3 and MN2 = 2). This has shifted the VTC of INV1 to the left and pushed VTC^{-1} of INV2 down making both the lobes of the butterfly curve wider with unequal sizes (since MN1 ≠ MN2). The SNM of CNFET-7T is higher than other two designs because its MN1 and MN2 have lower V_t which implies that switching threshold of both the inverters are lower than that of 6T and 7T.

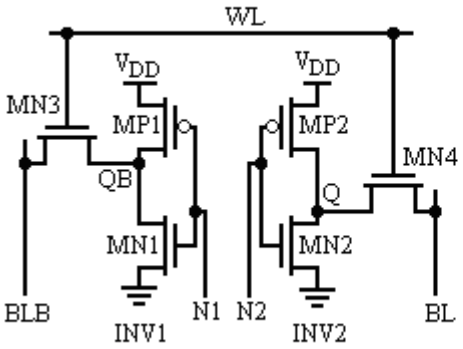

FIGURE 10. Test Setup for Measuring SNM of 6T.

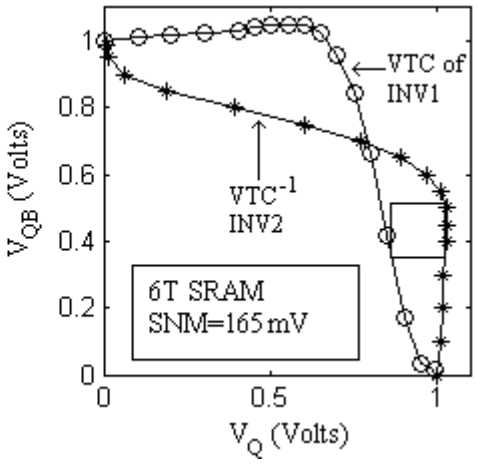

FIGURE 11. Static Noise Margin of 6T SRAM.

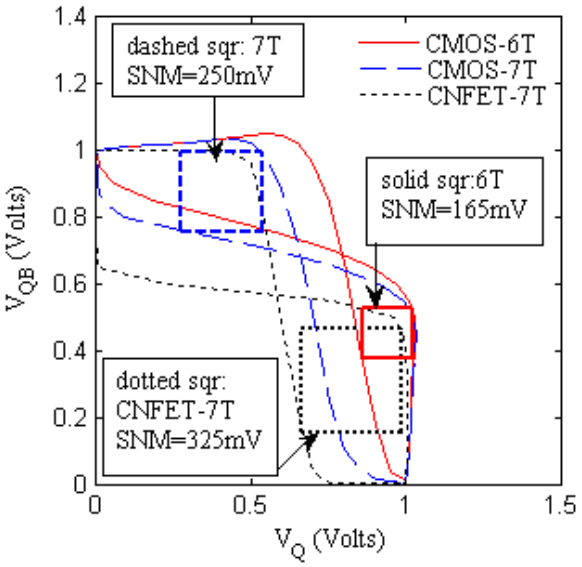

FIGURE 12. SNM of 6T, 7T and CNFET-7T SRAM Cell.

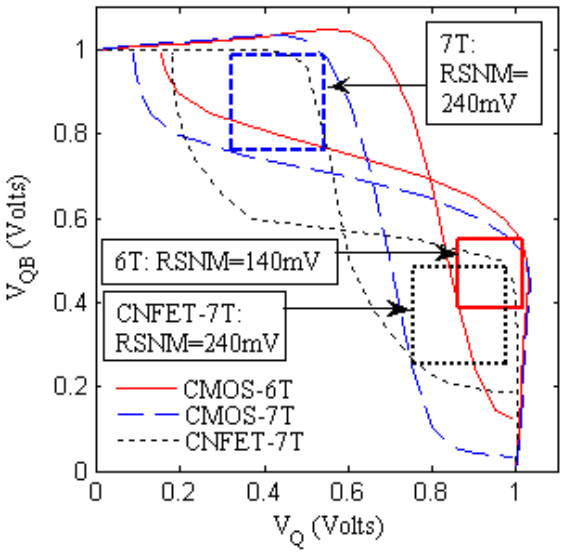

FIGURE 13. RSNM of 6T, 7T and CNFET-7T Cell.

5.3. Read Static Noise Margin Measurements

The SRAM cell is most vulnerable to noise during read access since the "0" storage node rises to a voltage higher than ground due to a voltage division along the access transistor and inverter pull-down NMOS driver. The ratio of the widths of the pull-down transistor to the access transistor, commonly referred to as the Cell Ratio (CR) or β ratio, determines how high the "0" storage node rises during a read access. Smaller cell ratios translate into a bigger voltage drop across the pull-down transistor, requiring a smaller noise voltage at the "0" storing node to trip the cell. RSNM is a measure of how much noise voltage is required at the node storing "0" to flip the state of an SRAM cell while reading. Therefore, RSNM is more critical design metric of SRAM cell than SNM. The RSNM of all the design are measured during simulation. Fig. 13 plots the RSNM of 6T, 7T and CNFET-7T. The plot shows that the 7T and CNFET-7T have RSNM ~240 mV and

outperform 6T in terms of 71.4% improvement in RSNM. This is attributed to the fact that both the inverters of 7T and CNFET-7T have stronger pull-down NMOS drivers that shift its VTC to the left and push VTC^{-1} down causing higher SNM compared to 6T. When VQB is increasing from 0, during read operation, DIBL impacts the Vts of transistors. This change in Vt also affects RSNM. All the results of noise margins are summarized in Table 5. The unequal size of the lobes of butterfly curves, particularly in 6T is due to unequal strength of MN1 and MN2. Though the aspect ratio of MN1 = 64 nm/64 nm = 1 and MN2 = 32 nm/32 nm = 1 their drive current differ, which is evident from Fig. 4. This is true for 7T also as its MN1 and MN2 are of unequal strength.

SNM type	6T	7T	CNFET- 7T
Hold SNM (mV)	165	250	325
RSNM (mV)	140	240	240

TABLE 5. Summary of Static Noise Margin.

5.4. Read Access Time and its Variability Measurements

Read delay is an important issue in high speed cache design. The variation of read delay is even more critical in scaled technology as it causes to fail to meet the deign budget. Therefore, this paper has focused to design SRAM cell immune to process variation. The T_{RA} measurements of 7T and CNFET-7T are taken with QB storing "0" and with QB storing "1" at V_{DD} = 1 V and at V_{DD} = 0.9 V. To assess the impact of PVT variations on T_{RA}, extensive Monte Carlo simulation is run applying ±3σ and ±10% Gaussian distribution on process parameters such as L (channel length), W (width), tox (oxide thickness), u0 (zero bias carrier mobility) and R□ (sheet resistance). The temperature is varied from 24 ℃ to 134 ℃ and the voltage is varied from nominal value of 1 V to 0.9 V (by −10%). The TRA (read access time) measurement results are presented in Table 6. The normalized values are reported in bracket. The increase in read delay (1.6× @ VDD = 1 V with QB storing "0") in proposed design is due to the reduced diameter of its pull-down drivers. The diameter reduction of drivers reduces their drive current which is evident from Fig. 4. As mentioned earlier, some of the parameters in SRAM cell are conflicting in nature. Improvement in some specific parameter is achieved only at the expense of other parameters. The read delay is a sacrifice to optimize other parameters. The TRA variability (σ/μ) of both the designs is estimated and compared. The estimated TRA variabilities are presented in Table 7. The normalized values are reported in bracket. Fig. 14 plots the normalized TRA variability. It is observed from the Table 7 and Fig. 14 that the proposed design offers 1.4× less spread in TRA at 1 V and 1.2× less spread in TRA at 0.9 V (with QB storing "0") than that of its counter part. This implies its robustness against PVT variations. This is attributed to the fact that the characteristic of CNFET is robust against PVT variation.

SRAM	Mean T_{RA} with QB storing "0" (ps)	Mean T_{RA} with QB storing "1" (ps)	V_{DD} (V)
7T	18.69(1)	16.99(1)	1
CNFET-7T	29.84(1.6)	23.51(1.4)	1
7T	25.41(1)	26.60(1)	0.9
CNFET-7T	34.15(1.3)	34.20(1.3)	0.9

TABLE 6. Read Access Time.

SRAM	T_{RA} variability (σ/μ) while QB storing "0"	V_{DD} (V)
7T	0.010(1.4)	1
CNFET- 7T	0.007(1)	1
7T	0.012(1.2)	0.9
CNFET-7T	0.010(1)	0.9

TABLE 7. Read Access Time Variability.

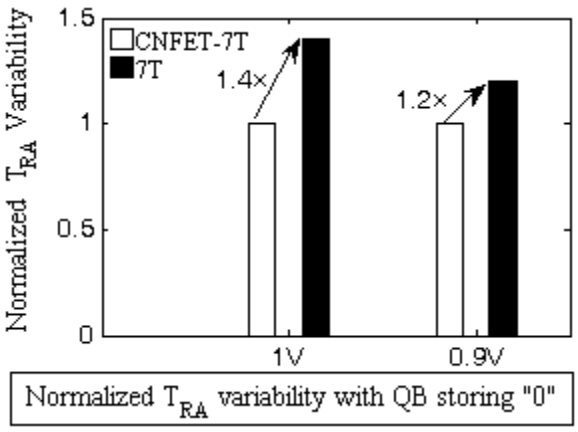

FIGURE 14. Normalized read Access Time Variability.

5.5. Write Access Time Measurements

The average TWA (write access time) is measured during simulation and results are tabulated in Table 8. The values of TWA are normalized with respect to that of CNFET-7T and the normalized values are reported in bracket. Fig. 15 plots the normalized values of TWA for making comparison easier. The Table 8 and Fig. 15 show that the CNFET-7T cell takes 1.3× and 1.2× less TWA, while writing "0" @ QB at VDD = 1 V and VDD= 0.9 V respectively. This difference in TWA occurs due to the difference in capacitance of storage node (say, CQB). The CQB mainly depends on drain diffusion capacitance of MN1, MP1 and MN5. The diffusion capacitance has two components per transistor – bottom-plate junction capacitance and side-wall junction capacitance as given by:

$$C_{diffusion} = C_j WL + C_{sw} X_j (W + 2L) \qquad (4)$$

where C_j is the junction capacitance per unit area, X_j is the junction depth, C_{sw} is the total (of three sides) side-wall junction capacitance per unit area, W and L are width and length of transistors. Equation (4) shows the W and L (area and perimeter) dependency of CQB. The MP1, MN1 and MN5 of 7T have larger area than corresponding transistors of CNFET-7T, giving rise to difference in bottom and three side-wall area and hence large difference in diffusion capacitance. This gives rise to longer difference in TWA. The write delay also depends on charging current, which in turn depends on supply voltage. Difference in write delay at VDD = 1 V and VDD = 0.9 V occurs due the same reason. Standard deviation of TWA is computed and reported in Table 9. The normalized values are reported in bracket and plotted in Fig. 16. Table 9 and Fig. 16 show that the spread of TWA of 7T is 1.4× and 1.2× wider than that of CNFET-7T while writing "0" @ QB at VDD= 1 V and 0.9 V respectively. This implies the robustness of proposed design with CNFET against PVT variation.

SRAM	T_{WA} while writing "0" @ QB (ps)	V_{DD} (V)
7T	24..02(1.3)	1
CNFET-7T	18.48(1)	1
7T	25.98(1.2)	0.9
CNFET-7T	21.65(1)	0.9

TABLE 8. Write Access Time.

SRAM	Standard Deviation (σ) of Write Access Time (T_{WA}) While writing "0" @ QB (ps)	V_{DD} (V)
7T	0.823(1.4)	1
CNFET-7T	0.588(1)	1
7T	0.932(1.2)	0.9
CNFET-7T	0.7774(1)	09

TABLE 9. Standard Deviation of Write Access Time

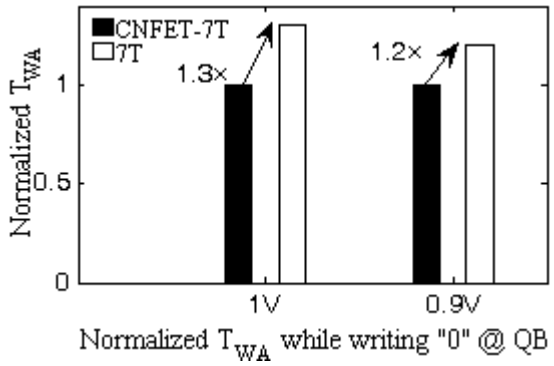

FIGURE 15. Normalized Write Access Time While Writing "0" @ QB.

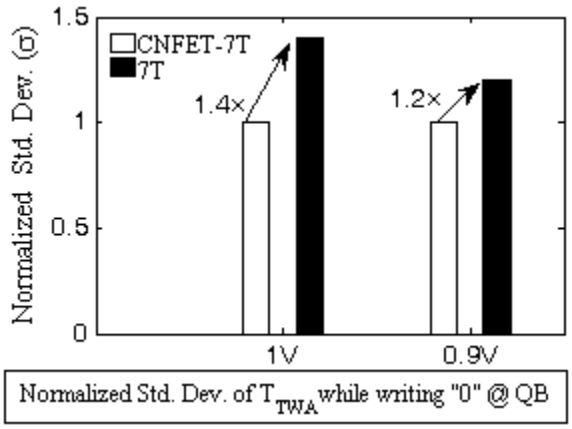

FIGURE 16. Normalized Standard Deviation of Write Access Time While Writing "0" @ QB.

6. CONCLUSION

This paper proposes CNFET-based 7T SRAM cell and analyzes the impact of process and temperature variations on read/write access time of CMOS-based 7T SRAM cell and CNFET-based 7T SRAM cell. All the simulations are performed at the nominal voltage of V_{DD} = 1V with –10% variations (i.e. at V_{DD} = 0.9V). The process parameters such as δL, δW, δt_{ox}, δu_0 and δRSH are varied by ±10% with relative and absolute Gaussian function during Monte Carlo simulation on HSPICE. The temperature is varied from 24℃ to 134℃ as well using absolute Gaussian function. Simulation measurements are taken for both the designs against $\pm 3\sigma$ variation of process parameters. It is observed during the investigation that the CNFET-based 7T SRAM cell is more robust against process variations compared to CMOS-based SRAM cell. This is due to the cylindrical geometry of CNFET. A variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNFET's operation. Moreover, the gate width in CNFET is not the effective channel width of the transistor. The paper has successfully demonstrated that the proposed design will be effective to reduce hold power, read delay variability, write delay and its variability.

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