Reducing Power Dissipation in FIR Filter: An Analysis

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Abstract

In this paper, three existing techniques, Signed Power-of-Two (SPT), Steepest decent and Coefficient segmentation, for power reduction of FIR filters are analyzed. These techniques reduce switching activity which is directly related to the power consumption of a circuit. In an FIR filter, the multiplier consumes maximum power. Therefore, power consumption can be reduced either by making the filter multiplier-less or by minimizing hamming distance between the coefficients of this multiplier as it directly translates into reduction in power dissipation [8]. The results obtained on four filters (LP) show that hamming distance can be reduced upto 26% and 47% in steepest decent and coefficient segmentation algorithm respectively. Multiplierless filter can be realized by realizing coefficients in signed power-of-two terms, i.e. by shifting and adding the coefficients, though at the cost of shift operation overhead.

Keywords: FIR, SPT, Steepest decent, Coefficient segmentation, low pass filter.

1. INTRODUCTION

The need for higher battery lifetime is ever increasing for portable devices like cellular phones, laptops, calculators, hearing aids and numerous other such devices. Due to large scale component integrations in such devices, power dissipation has become a major issue demanding special measures (heat sinks, special circuitry etc) to protect the chip from thermal runaway making the system complex and costly. So minimizing power dissipation of an application chip is a vital issue before researchers that needs to be addressed. In FIR filters, multipliers play an important role, and in a well designed CMOS circuit, switching component is a dominant term [5]. Input level transitions (0 to 1 or 1 to 0) are always associated with a power loss, which can be reduced by reducing toggling in the input of the multiplier. Power dissipation in a CMOS circuit is given as [5]

$P_{total} = P_{dynamic} + P_{short} + P_{leakage}$,

with $P_{dynamic} = \alpha.C_{load}.V^2_{dd}.f_{clk}$, $P_{short} = I_{sc}*V_{dd}$, and $P_{leakage} = I_{leakage}*V_{dd}$, where V_{dd} is the supply voltage, f_{clk} is the clock frequency, C_{load} is the load capacitance, α is the node transition factor i.e., the average number of 0 $\rightarrow$ 1 transitions for the equivalent electric node per clock cycle. I_{sc} and $I_{leakage}$ are the short circuit and leakage current respectively. This paper aims at reducing the switching factor, α, out of these factors while maintaining the throughput of the FIR filter.

2. RELATED WORK

Many methods have been reported for the reduction of power dissipation in FIR filter. Power reduction can be done at four levels- process, circuit, architectural, and algorithmic level. A multiplier in a FIR filter is most power consuming component and its implementation in VLSI is also very expensive. The coefficients of filter can be represented as sum of signed power-of-two terms making it multiplierless. Several algorithms are available for designing filters with signed power-of-two (SPT) coefficients [1-4, 12, 13]. Thus, multiplier can be replaced by adders and shifters, making the filter multiplierless. Also, adders can further be reduced by extracting common subexpressions from the coefficients [18].

Transition density of the inputs of multiplier can be reduced by minimizing hamming distance between the inputs [8, 11]. Mahesh Mehendale et. al. [9] presented seven transformations to reduce power dissipation which together operate at algorithmic, architectural, logic and layout levels of design abstraction. Power can be reduced by the way of arithmetic operators which use coding as a method of decreasing the switching activity [10]. In [14], the authors presented different architectures for implementation of low power FIR filtering cores. This included coefficient segmentation, block processing and combined segmentation and block processing algorithms. The work in [15] presents low power FIR filter implementations which are based on processing coefficients in a non-conventional order using both direct form and transposed direct form FIR filters.

3. FIR FILTER IMPLEMENTATION

FIR filters are widely used in digital signal processing (DSP) systems that are characterized by the extensive sequence of multiplication operations. These are also used in IF processing block of wireless communication systems. It can be represented by difference equation as given below:

$$y(n) = \sum_{k=0}^{M-1} h(k)\, x(n-k)$$

where h(k) are the coefficients of the filter, x(n) is the input , y(n) is the output and M is the order of the filter. Such a difference equation can be implemented using a transversal filter as shown in Fig 1. The transversal filter, which is also referred to as a tapped delay line filter, consists of three basic elements: (1) unit-delay element, (2) multiplier, and (3) adder. The number of delay elements used in the filter determines the finite duration of its impulse response. The number of delay elements, shown as M in Fig.1 is commonly referred as the filter order. The role of each multiplier in the filter is to multiply the tap input by a filter coefficient called tap weight.
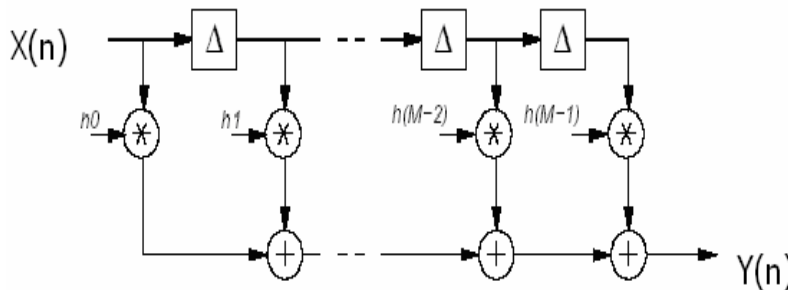

FIGURE 1: Transversal FIR Filter

4. SIGNED POWER-OF-TWO

The coefficients of fixed point FIR filter can be represented in sum of signed power-of-two (SPT) terms. In binary, multiply by 2 is implemented by simply shifting and adding the term. So in FIR, multiplier may be implemented by shifting the coefficients and then adding to input data. In this way, the power and complexity of multiplier can be minimized. As complexity of fixed point FIR filter is directly related to the number of total SPT terms[13], this number should be limited if complexity is also one of the constraint. The number of SPT terms per coefficient may be same. In the past decades, it has been shown that significant advantage can be achieved if the coefficient values are allocated with different number of SPT terms while keeping the total number of SPT terms for the filter fixed. Each coefficient value represented as a sum of signed power-of-two terms is given by the following equation [4]:

$$h(n) = \sum_{r=1}^{R} a(r)\, 2^{g(r)}$$

where a(r)=(-1, 0 or 1), h(n) is the nth coefficient value, g(r) is a positive integer and R is the number of terms.

The following algorithm [4] finds an approximation of a SPT term for a number x:

(i)   Initialize m = 1 and S_0 = x.

(ii) Find y(m)*$2^{g(m)}$ which minimizes | S_{m-1} - y(m)$2^{g(m)}$ |

(iii) If either y(m) = 0 or m = u, go to Step (vi), else
      go to Step (iv).

(iv) Update S_m = S_{m-1} - y(m)*$2^{g(m)}$

(v)   Increment m. Go to Step 2.

(vi) [x]u = $\sum_{i=1}^{M}$ y(i)*$2^{g(i)}$. Stop.

5. STEEPEST DECENT TECHNIQUE

Power dissipation can be reduced by minimizing the hamming distance between the coefficients of the filter by using steepest decent technique. It is a local search method in which a minima of the function can be found in its neighborhood. Hamming distance gives the measurement of the number of bit changes in the successive coefficients. As switching activity is proportional to hamming distance, it can be reduced by minimizing hamming distance. Algorithm for hamming distance minimization of FIR filters using steepest decent technique is as under [8]:

Step 1:- For a given FIR filter coefficients H[i] (i =1, N-1) and given pass band ripple and stop-
band attenuation, calculate the Hamming Distance between successive coefficients.

Step 2:- Now perturb each coefficient (increase the value of each coefficient one by one by 1)
and calculate new hamming distance between the coefficients H[i+], H[i-1] such that
HD(H[i], H[i-1]) > HD(H[i+], H[i-1])

Step 3:- Replace H[i] with H[i+] to get a new set of coefficients.

Step 4:- Now again perturb each coefficient (decrease the value of each coefficient one by one by
1)   and calculate new hamming distance between the coefficients H[i-], H[i-1] such that
HD(H[i], H[i-1]) > HD(H[i-], H[i-1])

Step 5:- Replace H[i] with H[i-] to get a new set of coefficients.

Step 6:- Compare the two sets and replace original coefficients with new value i.e. which having
smaller hamming distance.

Step 7:- Again compute hamming distance between new coefficients and also find pass band
ripple and stop band attenuation for this new set of coefficients.

Using this steepest decent strategy, for every coefficient, it's nearest higher and nearest lower coefficient values are identified. A new set of coefficient is formed by replacing one of the coefficients with it's nearest higher or nearest lower value i.e. having minimum hamming distance. Hamming distance is then calculated for this new set of coefficients. Also passband ripples and stopband attenuation is calculated.

6. COEFFICIENT SEGMENTATION

Using this algorithm, a coefficient is divided into two parts. For each coefficient the nearest signed power-of-two term is find and is subtracted from the original coefficient. This SPT term can be implemented using a shift operation and the rest of the coefficient value can be given to the multiplier in filter. In this way, the bits required to represent the coefficients becomes less. So the hamming distance between the successive coefficients, applied to multiplier, is reduced which in turn reduces switched capacitance. Hence, power consumption is reduced by reducing switching power. The main algorithm for segmentation is described as follow [11]:

Let H = (h_0, h_1,...., h_{N-1}), where N is the order of the filter. For a coefficient h_k, it is divided in such a way that h_k = s_k + m_k, where s_k is the component to be implemented using shift operation and the second component m_k is applied to the multiplier. To reduce the switched capacitance of the hardware multiplier, consecutive values of m_k, applied to the multiplier input must be of the same polarity, to minimize switching, and have the smallest value possible, to minimize the effective wordlength. In this case, m_k is chosen to be the smallest positive number. For a small positive m_k, s_k, must be the largest power of two number closest to h_k. So by

checking the polarity of h_k, if it is a positive number then s_k is chosen as the largest power of two number smaller then h_k. If it is negative, s_k is chosen as smallest power-of-two number larger than $|h_k|$. In both cases m_k is $h_k - s_k$.

7. RESULTS

The three algorithms (SPT, coefficient segmentation and steepest decent) were implemented under MATLAB environment on four different FIR low pass filters, with varying parameters (table 1) and number of coefficients. These filters were designed initially using window method. Coefficient values, obtained using these algorithms and quantized to 16-bit 2's complement representation form the initial set of coefficients for optimization. Hamming distance is first calculated for a particular set of coefficients using window method.

These coefficients are then calculated by using these algorithms and the hamming distance is recalculated. It is gathered from these results that upto 26% and 47% reduction in hamming distance is achievable using steepest decent and coefficient segmentation algorithm as shown in table 2. The passband ripple and stopband attenuation is also compared for all the cases as shown in table 3 and 4. Performance parameters degrade somewhat. The frequency response of filter 1 obtained for all the algorithms is shown in Fig. 2.

Filter	Passband (kHz)	Stopband (kHz)	Passband ripple (dB)	Stopband attenuation (dB)	Window function	Filter length
Filter 1	0-1.5	2-4	0.1	50	Hamming	53
Filter 2	0-1.2	1.7-5	0.01	40	Kaiser	71
Filter 3	0-1	1.5-5	0.0135	56	Kaiser	61
Filter 4	0-1.5	2-4	0.1	50	Blackman	89

TABLE 1: Low Pass Fir Filter Specifications

Filter	Initial Hamming Distance (HD)	Coefficient Segmentation		Steepest Decent	
		HD	Reduction (%)	HD	Reduction (%)
Filter 1	326	216	33.74	278	14.72
Filter 2	378	256	32.27	300	20.63
Filter 3	326	244	25.15	244	25.15
Filter 4	538	284	47.21	396	26.39

TABLE 2: Hamming distance obtained using these algorithms for different low pass filters

Filter	Performance parameters	Original	Coefficient Segmentation	Steepest Decent	SPT
Filter 1	Max (δp)	1.0042	1.0041	1.0044	1.0134
	Min (δp)	1.0000	1.0000	1.0001	1.0074
Filter 2	Max (δp)	1.0003	1.0002	1.0004	0.9937
	Min (δp)	0.9987	0.9987	0.9982	0.9919
Filter 3	Max (δp)	1.0012	1.0012	1.0056	1.0019
	Min (δp)	0.9985	0.9985	0.9833	0.9988
Filter 4	Max (δp)	1.0002	1.0001	1.0076	1.0127
	Min (δp)	0.9999	0.9998	0.9922	1.0085

TABLE 3: Comparison in terms of passband ripples

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Filter	Original	Coefficient Segmentation	Steepest Decent	SPT
Filter 1	-52	-52	-54	-43
Filter 2	-57	-57	-56	-45
Filter 3	-56	-56	-36	-40
Filter 4	-75	-75	-41	-46

TABLE 4: Comparison in terms of stopband attenuation(in db)

8. CONCLUSION

In this work, Signed power-of-two, Steepest decent and coefficient segmentation algorithms have been discussed for the low power realization of FIR filters. As, a multiplier is the major component for power dissipation, power can be reduced by minimizing the hamming distance between successive filter coefficients which are being fed to the multiplier. Steepest Decent optimization algorithm is presented so as to minimize the Hamming distance and the analysis shows that the total Hamming distance can be reduced upto 26%. But the penalty paid in this case is the degradation of performance parameters like. passband ripples and stopband attenuation. The results of coefficient segmentation shows that the hamming distance can be reduced upto 47%. Here the performance parameters are not degraded but an additional overhead, in terms of extra hardware and the power dissipated for shift and add operation, caused by shift operation is to be added. Also as reported in literature [11] power dissipation can be reduced considerably (63%) using SPT, as compared to these algorithms. However, the penalty is again in the form of additional overhead of adders and shifters. There exist a tradeoff between hamming distance reduction and degradation of performance parameters.
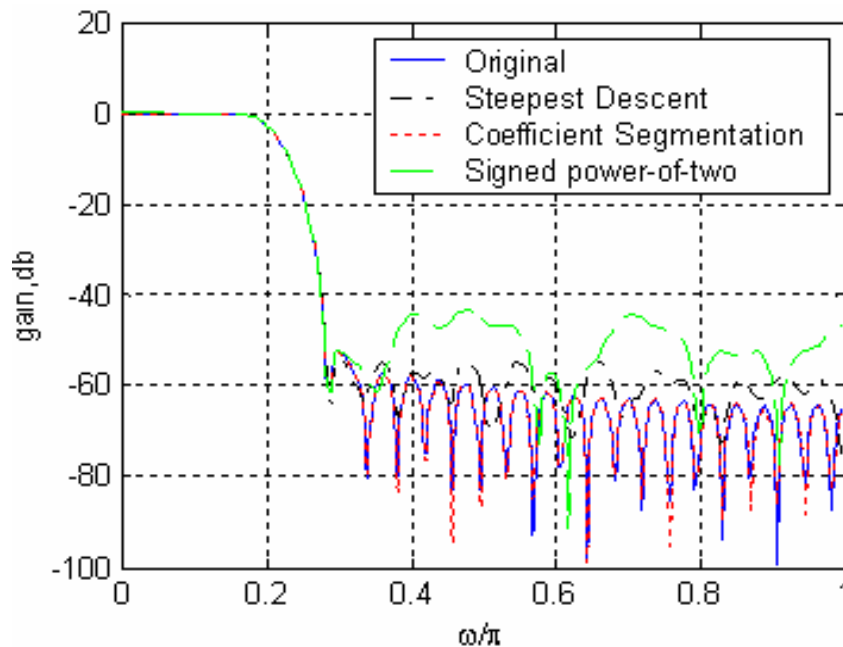

FIGURE 2: Frequency response of low pass FIR filter for example 1

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