Design of High Speed Low Power 15-4 Compressor Using Complementary Energy Path Adiabatic Logic

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Abstract

This paper presents the implementation of a novel high speed low power 15-4 Compressor for high speed multiplication applications using single phase clocked quasi static adiabatic logic namely CEPAL (Complementary Energy Path Adiabatic Logic). The main advantage of this static adiabatic logic is the minimization of the $1/2CVth^2$ energy dissipation occurring every cycle in the multi-phase power-clocked adiabatic circuits. The proposed Compressor uses bit sliced architecture to exploit the parallelism in the computation of sum of 15 input bits by five full adders. The newly proposed Compressor is also centered around the design of a novel 5-3 Compressor that attempts to minimize the stage delays of a conventional 5-3 Compressor that is designed using single bit full adder and half adder architectures. Firstly, the performance characteristics of CEPAL 15-3 Compressor with 14 transistor and 10 transistor adder designs are compared against the conventional static CMOS logic counterpart to identify its adiabatic power advantage. The analyses are carried out using the industry standard Tanner EDA design environment using 250 nm technology libraries. The results prove that CEPAL 14T 15-4 Compressor is 68.11% power efficient, 75.31% faster over its static CMOS counterpart.

Keywords: Compressor; Static Adiabatic Logic, CEPAL (Complementary Energy Path Adiabatic Logic), Multi-phase Power-clocked Adiabatic Circuits .

1. INTRODUCTION

With the advancement in CMOS technology, chip capacity (transistor count) and clock frequencies have increased. As a result, the power dissipation of digital CMOS design has skyrocketed and now is a primary design constraint.[1] In the past, due to a high degree of process complexity and the exorbitant costs involved, low power circuit design was used in applications where very low power dissipation was absolutely essential, but now it became the norm for all high-performance applications.[2] So, low power techniques are highly appreciated in current VLSI design.

This has motivated the designers to explore various design approaches to reduce power dissipation in VLSI circuits. Adiabatic logic has been applied to low-power systems, and several adiabatic logic families have been proposed for low power applications [3]–[8]. Energy recovery circuits based on the adiabatic logic have been proved to be a promising approach among non-conventional low power design methodologies. The primary advantage of adiabatic circuits results

from its inherent nature of deriving a constant current from the appropriately called power-clock sources and making the FET switches function with minimum voltage across the source and drain [9].

There are several types of static adiabatic logic circuits, namely, Complementary Energy Path Adiabatic Logic (CEPAL), Quasi Static Energy Recovery Logic (QSERL) and Quasi Static Single-phase Energy Recovery Logic (QSSERL). They are all designed to overcome the drawbacks of the previously available irreversible adiabatic logic styles. These adiabatic circuits use sinusoidal power clock sources for operation. Since the sinusoidal power-clock generation has been proved versatile, it makes them suitable for energy recovery circuits as against the adiabatic logic styles employing trapezoidal or triangular power clock pulses.

Multiplication is the basic arithmetic operation in several microprocessors and digital signal processing applications. Digital Signal Processing systems require multipliers to implement DSP algorithms such as convolution and filtering where the multiplier lies directly within the critical path. Hence, the demand for high speed multipliers has become prominent. The enhanced speed leads to increased power dissipation, thus, power saving architectures turn to be the choice of the future. This has given way to the development of novel circuit techniques, with the aim of reducing the power dissipation of multipliers without compromising the speed and performance.

The earliest reported multiplier was an array multiplier that uses a chain of ripple carry adders to compute the product by means of repetitive addition [10]. Multiplier architecture is essentially divisible into three stages: a partial product generation stage, a partial product addition stage and final addition stage. A fast array or tree multiplier is composed of three sub-circuits: a Booth encoder for generation of partial products, a carry save structured accumulator for summing up the partial products and a final carry propagation adder to compute the final binary result from its stored carry representation [11]. The second stage requires the use of adders or Compressors and this stage mainly contribute to delay and power. Therefore speeding up the second stage and lowering its power dissipation are the most eminent means of achieving performance improvement of the multiplier. In high speed multipliers, 4-2 Compressors are widely used to lower the latency of the partial product accumulation stage. 4-2 compression is ideal for constructing regularly structured Wallace tree with low complexity. However, for the compression of a larger number of bits, higher orders Compressors are needed.

Section II gives an introduction to CEPAL. The proposed structure of 5-3 Compressor is given in Section III. The proposed structure of 15-4 Compressor and the details on how to implement it using CEPAL logic style is presented in the two subsequent sections. Experimental results are given in Section VI, and this paper is concluded in Section VII.

2. COMPLEMENTARY ENERGY PATH ADIABATIC LOGIC

The structure of the static energy recovery logic CEPAL is shown in Fig 1. CEPAL uses two complementary sinusoidal power clocks. The CEPAL consists of two transistors, Pull-up and Pull down networks charging and discharging transistors as seen in Fig. 1. Let us understand the operation of the circuit. Let us assume that the initial output V_{out} is high, and the Pull up network is on, while the Pull down network is off, the output node will neither be following the power clock PC nor its complement PC_{bar}, when the next input does not warrant a change in the output node.

Let us consider the alternate case, in which, the initial output V_{out} is low and the Pull up network is on, while the Pull down network is off. Then, the output node V_{out} follows either PC or its compliment PC_{bar}, whichever swings to high level. Once the output reaches high, it ramps down to low level following the power clock during its downward transition, thus making the node V_{out} to become a floating node. However, this condition is overcome when the compliment of the power clock swings to high level. This eliminates the weak high node and also eliminates the hold state of the two phase power clock operated circuits.

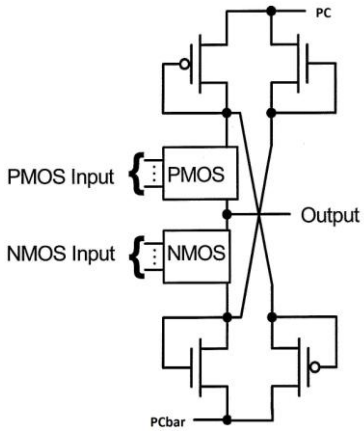

FIGURE 1: Complementary Energy Path Adiabatic Logic.

3. STRUCTURE AND DESIGN OF 5-3 COMPRESSOR

3.1 Half adder

The half adder adds two single binary bits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The input variables of a half adder are called the augend and addend bits. The carry signal represents an overflow into the next digit of a multi-digit addition. The simplest half-adder design incorporates an XOR gate for *S* and an AND gate for *C*. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The structure of half adder is shown in the below figure.

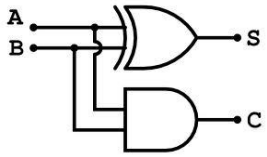

FIGURE 2: Logic Design of Half Adder.

The number of transistors and the average power of the Half Adder using CMOS and CEPAL are shown in Table 1.

Logic	P-MOS	N-MOS	Total Transistors	Average Power (μW)
CMOS	9	9	18	33.79
CEPAL	19	19	38	11.66

TABLE 1: Half Adder Transistor count & Power Comparison.

The CEPAL Half adder is 65.49% more power efficient as compared to its CMOS counterpart. Figure 3 shows the output waveforms of the CEPAL Half adder, where PC and PCbar are the two complementary power clocks. The plot p(VVoltageSource_4) shows the power dissipation of the power clock.

FIGURE3: Output waveforms of Half Adder.

3.2 Full adder

A full adder adds binary bits and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in}; A and B are the operands, and C_{in} is a bit carried in from the next less significant stage. The full-adder is usually a component in a cascade of adders. The circuit produces a two-bit output, that is, output carry and sum typically represented by the signals C_{out} and S. The structure of half adder is as shown in the below figure.

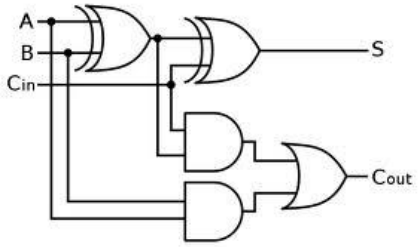

FIGURE 4: Logic Design of Full Adder.

The number of transistors and the average power of the Full Adder using CMOS and CEPAL are shown in Table 2.

Logic	P-MOS	N-MOS	Total Transistors	Average Power (µW)
CMOS	27	27	54	66.86
CEPAL	59	59	118	31.26

TABLE 2: Full Adder Transistor count & Power Comparison.

The CEPAL Full Adder is found to be 53.25% power efficient as compared to the counterpart in CMOS technology. Figure 5 shows the output waveforms of the CEPAL Full Adder. Plot PC and PCbar show the power clock given. The plot p(VVoltageSource_4) shows the power consumption of the power clock.

FIGURE 5: Output waveforms of Full Adder.

3.3 Architecture of 5-3 Compressor

A 5-3 Compressor comprises of a combinational logic circuit with five inputs and three outputs. It accepts a five bit input string, and produces its sum as output. The maximum output of a 5-3 Compressor can be 101, when all its input bits are at logic 1. The conventional architecture of a 5-3 Compressor is based on the design of a conventional 4-2 Compressor. The architecture of a conventional 5-3 Compressor is shown in figure 1.

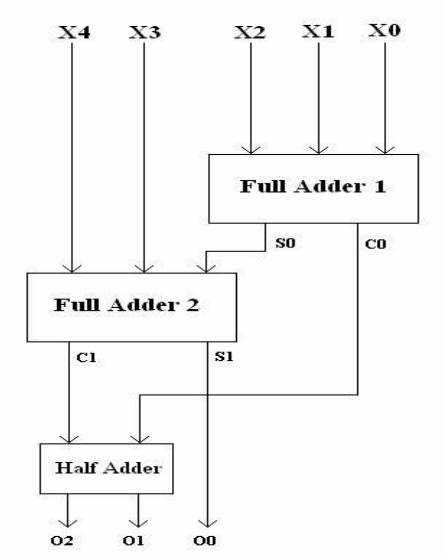

FIGURE 6: Architecture of conventional 5-3 Compressor.

As evident from the figure 6, the implementation of the 5-3 Compressor has for 5 gate delays. Moreover the least significant bit of the output requires 4 gate delays (delay imposed by four XOR gates). As a result, there can be a problem of synchronization of the output bits when the input bits change leading to static hazards. We propose a novel architecture of a 5- 3 Compressor that can produce output with only three gate delays. The architecture of the Compressor has been obtained by suitably rewriting the Boolean equations of a 5-3 Compressor as:

$$O_0 = x_0 \oplus x_1 \oplus x_2 \oplus x_3 \oplus x_4 \quad (1)$$

$$O_1 = \left((x_0 \oplus x_1 \oplus x_2 \oplus x_3).x_4\left(\overline{x_0 \oplus x_1 \oplus x_2 \oplus x_3}\right).x_3\right) \oplus \left((x_0 \oplus x_1).x_2 + \left(\overline{x_0 \oplus x_1}\right).x_0\right) \quad (2)$$

$$O_2 = \left((x_0 \oplus x_1 \oplus x_2 \oplus x_3).x_4\left(\overline{x_0 \oplus x_1 \oplus x_2 \oplus x_3}\right).x_3\right).\left((x_0 \oplus x_1).x_2 + \left(\overline{x_0 \oplus x_1}\right).x_0\right) \quad (3)$$

Using equations (1), (2) and (3), we propose to design a multiplexer based architecture of a 5-3 Compressor as shown in figure 7.

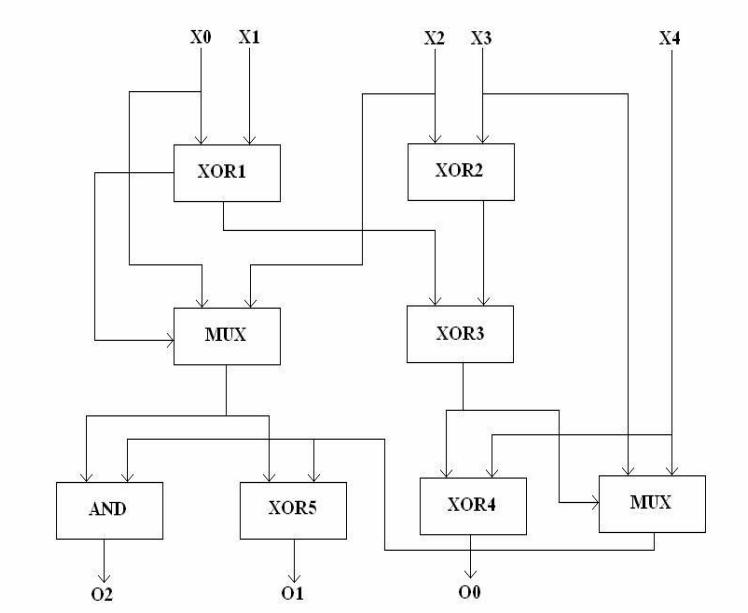

FIGURE 7: Architecture of proposed 5-3 Compressor.

It is evident from Fig. 7, that the output of the Compressor requires 3 gate delays. It is therefore obvious that the proposed 5-3 Compressor computes the compressed output with a much lesser delay than the conventional 5-3 Compressor.

The number of transistors and the average power of the 5-3 Compressor using CMOS and CEPAL are shown in Table 3.

Logic	P-MOS	N-MOS	Total Transistors	Average Power (µW)
CMOS	45	45	90	74.64
CEPAL	91	91	182	41.84

TABLE 3: 5-3 Compressor Transistor count & Power Comparison.

There is an increase in the number of transistors in the CEPAL technology; nevertheless, there is a significant decrease in power. The CEPAL 5:3 Compressor is 43.94% more power efficient as compared to its CMOS counterpart. Figure 8 shows the output waveforms of the CEPAL 5:3 Compressor, where PC and PCbar are the two complementary power clocks. The plot p(VVoltageSource_10) shows the power dissipation of the power clock.

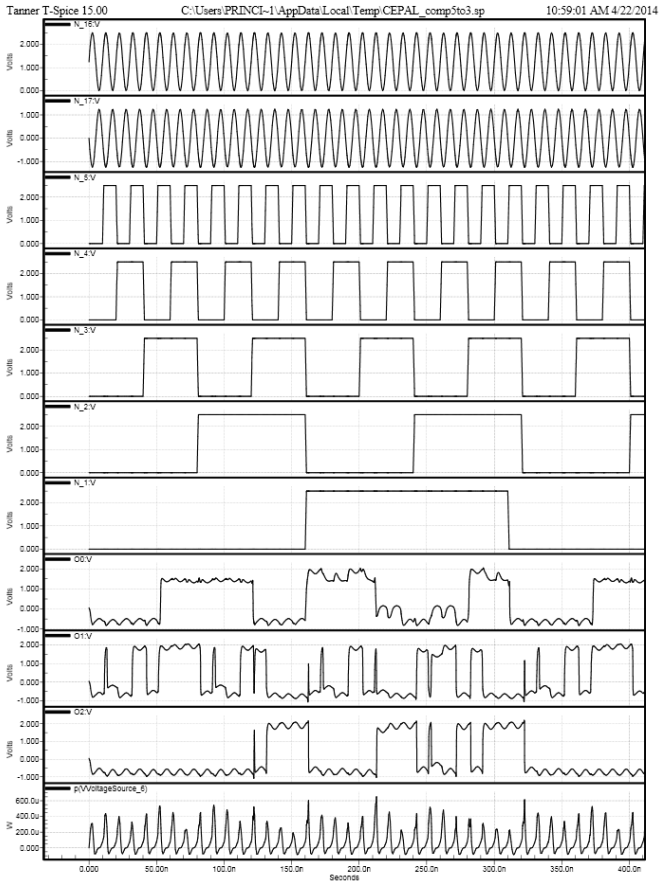

FIGURE 8: Output waveforms of proposed 5-3 Compressor.

4. ARCHITECTURE OF 15-4 COMPRESSOR

15-4 Compressor has been designed using the proposed 5-3 Compressor. The architectural design of the proposed 15-4 Compressor is shown in figure 9. The architecture is based on a bit sliced addition technique. The 15 input bits are divided five groups of three bits each. The 3 input bits in each group are compressed into 2 bits in the first stage using a full adder. The sum and carry outputs of each adder are thereafter sent to two 5-3 Compressors whose design has been discussed in section 3. The outputs of the Compressor are sent to a 4 bit parallel adder that has been suitably optimized according to the design requirements.

Since the 5-3 Compressor that computes the sum of the carry outputs of the full adders in the first stage produces a result that has twice the weight of the output of the other Compressor, hence the Compressor output is sent to the parallel adder after being appropriately left shifted. Since least significant bit of the one set of 4 bits is zero and the most significant bit of the other set of 4 bits is zero, hence the adder design is suitably optimized as shown in figure 10.

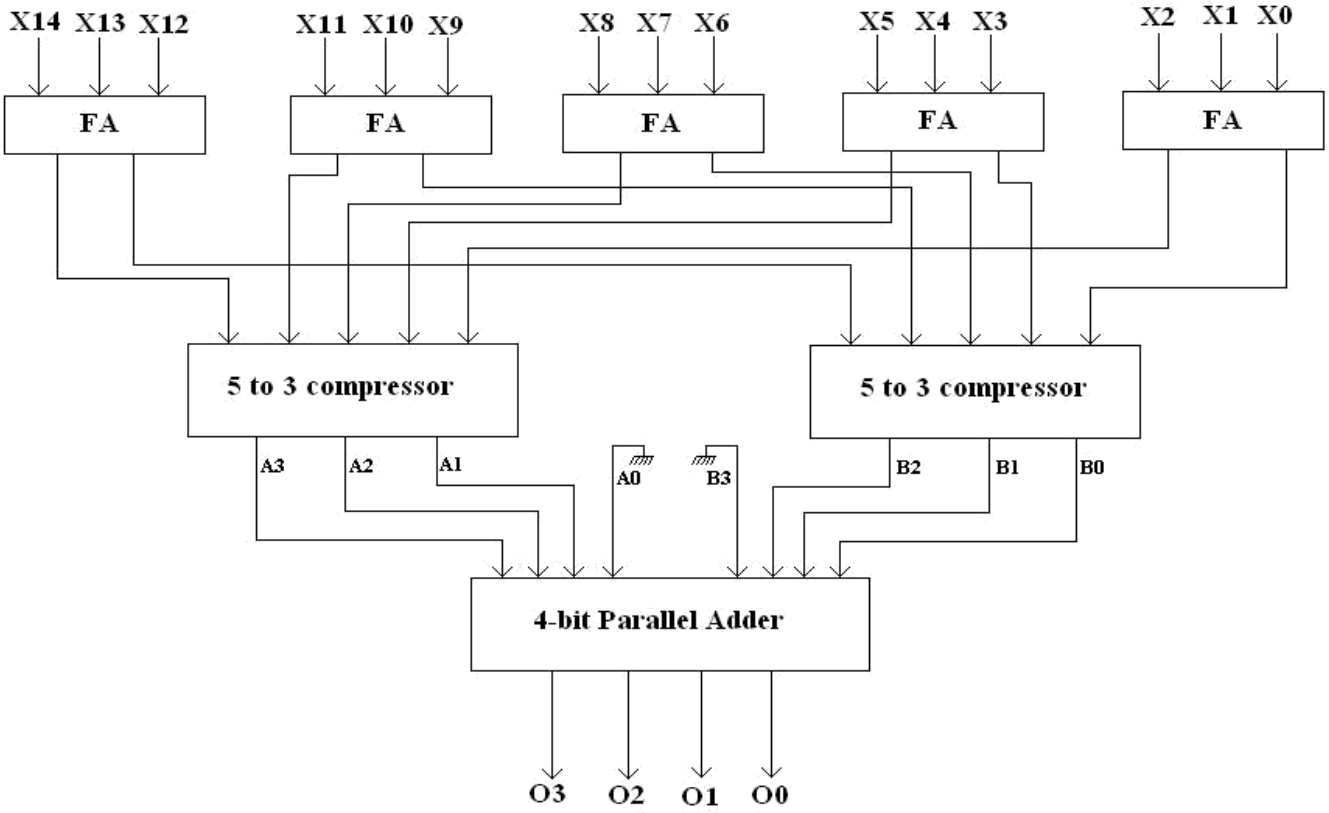

FIGURE 9: Architecture of proposed 15-4 Compressor.

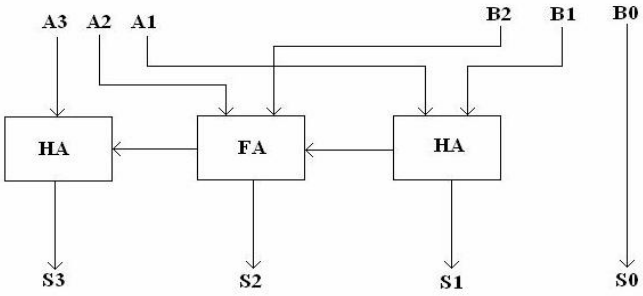

FIGURE 10: Optimal design of Parallel adder.

5. CIRCUIT DESIGN OF 15-4 COMPRESSOR

The circuit has been designed, simulated and tested using 10 transistor [12] and 14 transistor [13] adder circuits. The design of the 10 transistor adder and 14 transistor adder are shown in figure 11(a) and 11(b) respectively.

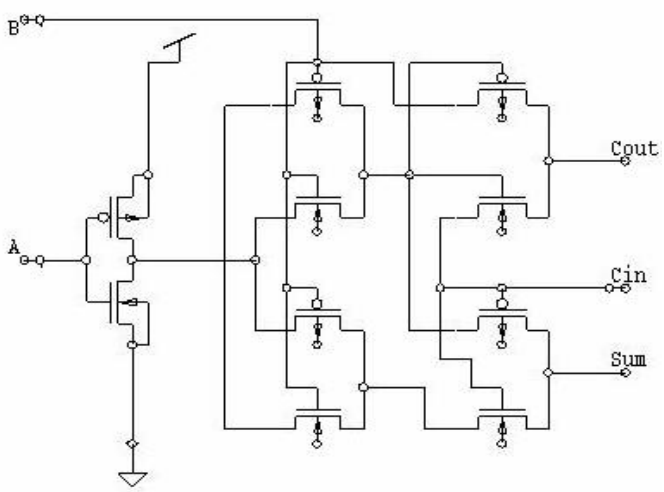

FIGURE 11 (a): Design of 10T adder.

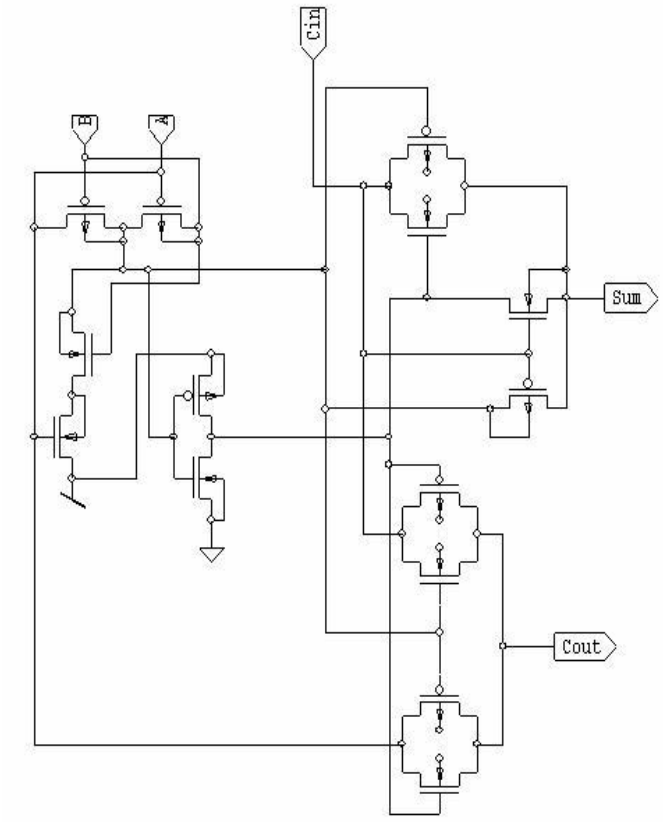

FIGURE 11 (b): Design of 14T adder.

6.RESULTS

The CEPAL (Complementary Energy Path Adiabatic Logic) based 15-4 Compressor is implemented using 250nm technology of the Tanner EDA with a W/L = 0.35µm/0.25µm and at 2.5V operating voltage along with a power clock frequency of 100MHz.

The number of transistors and the average power of the 15-4 Compressor using CMOS and CEPAL are shown in Table 4.

Logic	P-MOS	N-MOS	Total Transistors	Average Power (µW)	Delay (ps)	PDP (pJ)
CMOS based 10T adder design	160	160	320	261.14	549.67	0.144
CMOS based 14T adder design	170	170	340	349.17	536.31	0.187
CEPAL based 10T adder design	252	252	504	165.74	217.67	0.036
CEPAL based 14T adder design	262	262	524	111.35	135.70	0.015

TABLE 4: 15-4 Compressor Transistor count & Power Comparison.

The CEPAL 15-4 Compressor is found to be 68.11% power efficient, 75.31% faster as compared to its CMOS counterpart; this added advantage is a well worth tradeoff for the increased transistor count.

A comparative study of the simulation results presented in the above table indicates that the 14T adder based design is more efficient in terms of power, delay and power-delay product, although the circuit area becomes somewhat more compared to its 10T adder based counterpart.

7. CONCLUSION

In this paper, we have presented the implementation of 15-4 Compressor circuit using single phase adiabatic logic family, namely, CEPAL (Complementary Energy Path Adiabatic Logic). The CEPAL uses increased number of transistors than the CMOS logic style due to the necessity of using the MOS diodes, in the charging/discharging process paths. These MOS diodes used in the CEPAL structure makes it identified as a static logic and the use of diodes helps in reducing the switching activity. The CEPAL structure, being a static type of logic, incurs the reduced switching activity.

The newly proposed Compressor is also centered around the design of a novel 5-3 Compressor that attempts to minimize the stage delays of a conventional 5-3 Compressor that is designed using single bit full adder and half adder architectures. The proposed 15-4 Compressor uses the minimum number of hardware resources so far as the logic level architecture of the design is concerned.

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